4-4-00

JC780 U.S. PTO
04/03/00

NEW, CONTINUATION, DIVISIONAL OR
CONTINUATION-IN-PART APPLICATION
UNDER 37 C.F.R. §1.53(b)

Attorney Docket No. 9329-001COL

JC525 U.S. PTO
09/541285
04/03/00

Express Mail Label No. EJ 568 510 235 US

Date March 31, 2000

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Hon. Commissioner of Patents and Trademarks
Washington, D. C. 20231

Sir:

Transmitted herewith for filing under 37 C.F.R §1.53(b) is a patent application for

**ELECTRONIC STILL VIDEO CAMERA WITH DIRECT PERSONAL COMPUTER (PC) COMPATIBLE DIGITAL FORMAT OUTPUT**

identified by: [ X ] First named inventor: **Marc K. Roberts**
or [ X ] Attorney Docket No. (see above)

1. **Type of Application**

[ ] This application is a new (non-continuing) application.

[ X] This application is a [ X] continuation of prior application No. **08/651,562, filed May 22, 1996.** Amend the specification by inserting before the first line the sentence:

> **--This is a continuation of United States patent application No. 08/651,562, filed May 22, 1996, which is a continuation of U.S. patent application No. 08/098,787** filed **July 29, 1993, which is a continuation of U. S. patent application No. 07/878,603, filed May 5, 1992, now abandoned, which is a continuation of United States patent application Serial No. 07/615,848, filed November 20, 1990 and now U.S. Patent No. 5,138,459. --**

[ X ] The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied, is considered part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

If for some reason applicant has not requested a sufficient extension of time in the parent application, and/or has not paid a sufficient fee for any necessary response in the parent application and/or for the extension of time necessary to prevent the abandonment of the parent application
prior to the filing of this application, please consider this as a Request for an Extension for the required time period and/or authorization to charge our Deposit Account No. 08-0750 for any fee that may be due. THIS FORM IS BEING FILED IN TRIPLICATE: one copy for this application; one copy for use in connection with the Deposit Account (if applicable); and one copy for the above-mentioned parent application (if any extension of time is necessary).

2. **Contents of Application**

a. Specification of 27 pages;
[ ] A microfiche computer program (Appendix);
[ ] A nucleotide and/or amino acid sequence submission;

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[ X ] Cancel original claims **2-20** of the prior application before calculating the filing fee. (At least one original independent claim must be retained for filing date purposes.)

b. [ X ] Drawings on **11** sheets;

c. [ X ] A signed Oath/Declaration [ X ] is enclosed / [ ] will be filed in accordance with 37 C.F.R. §1.53(f).

The enclosed Oath/Declaration is [ ] newly executed / [ X ] a copy from a prior application under 37 C.F.R. §1.63(d) / [ ] accompanied by a statement requesting the deletion of person(s) not inventors in the continuing application.

d. **Fees**

| **FILING FEE CALCULATION** | Number Filed | | Number Extra | | Rate | | Basic Fee $690.00 |
|---|---|---|---|---|---|---|---|
| Total Claims | 16 - | 20 = | -0- | × | $18.00 | = | -0- |
| Independent Claims | 8 - | 3 = | 5 | × | $78.00 | = | $390.00 |
| Multiple Dependent Claim(s) Used | | | | | $260.00 | = | -0- |
| FILING FEE - NON-SMALL ENTITY | | | | | | | $1,080.00 |
| FILING FEE - SMALL ENTITY: Reduction by 1/2<br>[ ] Verified Statement under 37 C.F.R. §1.27 is enclosed.<br>[ ] Verified Statement filed in prior application. | | | | | | | |
| Assignment Recordal Fee ($40.00) | | | | | | | |
| 37 C.F.R. §1.17(k) Fee (non-English application) | | | | | | | |
| **TOTAL** | | | | | | | **$1,080.00** |

[ X ] A check is enclosed to cover the calculated fees. The Commissioner is hereby authorized to charge any additional fees that may be required, or credit any overpayment, to Deposit Account No. 08-0750. A duplicate copy of this document is enclosed.

[ ] The calculated fees will be paid within the time allotted for completion of the filing requirements.

[ ] The calculated fees are to be charged to Deposit Account No. 08-0750. The Commissioner is hereby authorized to charge any additional fees that may be required, or credit any overpayment, to said Deposit Account. A duplicate copy of this document is enclosed.

3. **Priority Information**

[ ] **Foreign Priority**: Priority based on _____ Application No. _____, filed _____, is claimed.

Attorney Docket No. 9329-001COL

Express Mail Label No. EJ 568 510 235 US

Date March 31, 2000

4. **Other Submissions**

[ **X** ] A Preliminary Amendment is enclosed.

[ **X** ] An Information Disclosure Statement is enclosed.

[ **X** ] A power of attorney

[ ] is submitted [ ] with the new Oath/Declaration.

[ **X** ] is of record in the prior application and [ **X** ] is in the original papers / [ **X** ] a copy is enclosed.

[ **X** ] An Assignment of the invention

[ ] is enclosed with a cover sheet pursuant to 37 C.F.R. §§3.11, 3.28 and 3.31.

[ **X** ] is of record in a prior application. The assignment is to **St. Clair Intellectual Property Consultants, Inc.**, and is recorded at Reel **7803**, Frame(s) **0944**.

[ ] An Establishment of Assignee's Right To Prosecute Application Under 37 C.F.R. §3.73(b), and Power Of Attorney is enclosed.

[**X** ] An Express Mailing Certificate is enclosed.

[ **X** ] Other: **Check covering additional claim fee.**

Attention is directed to the fact that the correspondence address for this application is:

Harness, Dickey & Pierce, P.L.C.
P.O. Box 828
Bloomfield Hills, Michigan 48303
(248) 641-1600.

Respectfully,

Date April 3, 2000

Gordon K. Harris, Jr.
Reg. No. 28,615

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{Applns.new\9329\001COL.Rule53B.APP.doc}

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Hon. Commissioner of Patents
and Trademarks
Washington, D.C. 20231

Sir:

**EXPRESS MAILING CERTIFICATE**

Applicant: **Marc K. Roberts, Matthew A. Chikosky, Jerry A. Speasl**

Serial No. (if any): unknown
(Continuation application under 37 C.F.R. §1.53(b) of U.S. Serial No. 08/651,562, filed May 22, 1996)

For: **ELECTRONIC STILL VIDEO CAMERA WITH DIRECT PERSONAL COMPUTER (PC) COMPATIBLE DIGITAL FORMAT OUTPUT**

Docket: **9329-001COL**

Attorney: **Gordon K. Harris, Jr.**

**"Express Mail" Mailing Label Number.....EJ 568 510 235 US**

**Date of Deposit.....April 3, 2000**

I hereby certify and verify that the accompanying **Request for continuation application under 37 C.F.R. §1.53(b), filed in triplicate; copy of originally filed prior application including Declaration; 11 sheets of formal drawings; Preliminary Amendment (8 pages); Information Disclosure Statement; and a Check in the amount of $1,080.00 for government filing fee** are being deposited with the United States Postal Service "Express Mail Post Office To Addressee" service under 37 C.F.R. 1.10 on the date indicated above and is (are) addressed to the Commissioner of Patents and Trademarks, Washington, D.C. 20231.

Date: April 3, 2000

Joan M. Oleksa

Applicant or Patentee: Roberts et al.
Serial or Patent No.: 07/878,603
Filed or Issued: May 5, 1992
Attorney's Docket No.:
Title: ELECTRONIC STILL VIDEO CAMERA WITH DIRECT PERSONAL COMPUTER (PC) COMPATIBLE DIGITAL FORMAT OUTPUT

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS
(37 CFR 1.9(f) & 1.27(c))--SMALL BUSINESS CONCERN

I hereby declare that I am

☐ the owner of the small business concern identified below:
☒ an official of the small business concern empowered to act on behalf of the concern identified below:
NAME OF SMALL BUSINESS CONCERN PC Camera Inc.
ADDRESS OF SMALL BUSINESS CONCERN McLean, Virginia 22013

I hereby declare that the above identified small business concern qualifies as a small business concern as defined in 13 CFR 121.12, and reproduced in 37 CFR 1.9(d), for purposes of paying reduced fees to the United States Patent and Trademark Office, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

I hereby declare that rights under contract or law have been conveyed to and remain with the small business concern identified above with regard to the invention, entitled ELECTRONIC STILL VIDEO CAMERA WITH DIRECT PERSONAL COMPUTER (PC) COMPATIBLE DIGITAL FORMAT OUTPUT by Roberts et al. by inventor(s) described in

☐ the specification filed herewith
☒ application serial no. 07/878,603, filed May 5, 1992
☐ patent no. _____, issued _____.

If the rights held by the above identified small business concern are not exclusive, each individual, concern or organization having rights in the invention is listed below* and no rights to the invention are held by any person, other than the inventor, who would not qualify as an independent inventor under 37 CFR 1.9(c) if that person made the invention, or by any concern which would not qualify as a small business concern under 37 CFR 1.9(d), or a nonprofit organization under 37 CFR 1.9(e). *NOTE: Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)

NAME PC Camera Inc.
ADDRESS McLean, Virginia 22013
☐ INDIVIDUAL ☒ SMALL BUSINESS CONCERN ☐ NONPROFIT ORGANIZATION

NAME _____
ADDRESS _____
☐ INDIVIDUAL ☐ SMALL BUSINESS CONCERN ☐ NONPROFIT ORGANIZATION

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

NAME OF PERSON SIGNING Joseph W. Conroy
TITLE OF PERSON IF OTHER THAN OWNER Corporate Secretary
ADDRESS OF PERSON SIGNING PC Camera Inc.
8330 Boone Blvd., Suite 550
Vienna, Virginia
SIGNATURE Joseph W. Conroy DATE 1/12/93

Attorney Docket No.9329-0001COL

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

*PATENT*

| | |
|---|---|
| 37 C.F.R. §1.53(b) Continuation of Marc K. Roberts et al.<br><br>Application Serial No. unknown (Continuation appln. of USSN 08/651,562, filed May 22, 1996)<br><br>Filed: concurrently herewith<br><br>For: ELECTRONIC STILL VIDEO CAMERA WITH DIRECT PERSONAL COMPUTER (PC) COMPATIBLE DIGITAL FORMAT OUTPUT<br><br>Attorney Docket No.: 9329-001COL | PRELIMINARY<br><br>AMENDMENT |

Hon. Commissioner of Patents and Trademarks,
Washington, D.C. 20231

SIR:

Prior to examination of the captioned continuation application filed pursuant to 37 C.F.R. §1.53(b), please amend the application, as follows:

IN THE CLAIMS:

Please cancel claim 1 and add the following new claims:

21. (NEW) A process for storing a digitized version of data corresponding to an image captured by an electronic camera, the process comprising:

storing in a selectively addressable memory in the camera at least one of a plurality of different digital data file format codes, each code corresponding respectively to at least one of a plurality of different data file formats for different types of computer apparatus,

formatting in the camera the digitized version of a captured image in accordance with a selected digital data file format code, and

storing the formatted digitized version in a digital memory directly coupled to the camera.

22. (NEW) The process of Claim 21 further comprising the preliminary steps performed in the camera of:

checking the format of the digital memory for compatibility with a predetermined type of information handling device, and

performing memory format initialization of the digital memory whenever compatibility with the information handling device is not found.

23. (NEW) The method of Claim 21 wherein the digital memory is removably coupled to the camera.

24. (NEW) The method of Claim 21 wherein the digital memory comprises a memory element normally associated with a personal computer.

25. (NEW) A video image signal data format translator comprising:

a translator housing:

an input interface in the translator housing for removable receipt of a first memory element containing a first electrical representation of a captured image:

a converter coupled to the input interface and operative to convert the first electrical representation into a second electrical representation;

an output interface in the translator housing for removable receipt of a second memory element normally usable in conjunction with an information handling device; and

a stored program controller in the translator housing operative to arrange the second electrical representation in a preselected format and to present the formatted second electrical representation to the output interface for storage in a second memory element, the format being directly compatible with a program running on the information handling device.

26. (NEW) The translator of Claim 25 wherein the stored program controller is further operative to check the format of a second memory element coupled to the output interface for agreement with the preselected format and to perform initialization of the second memory element whenever agreement with the preselected format is not found.

27. (NEW) The translator of Claim 25 wherein the input interface can removably receive a first memory element comprising an analog video memory element, the output interface can removably receive a second memory element comprising a digital memory element, and the converter includes an analog to digital converter.

28. (NEW) A method of translating in a signal format translator a first electrical representation of a video image signal into a second electrical representation of the video image signal for storage in an output memory element, the method comprising:

reading the first electrical representation from an input memory element coupled to the translator and presenting the first electrical representation to a converter located in the translator;

converting the first electrical representation into the second electrical representation using the converter;

determining in the translator a preselected format for the second electrical representation;

formatting in the translator the second electrical representation in accordance with the preselected format; and

writing the formatted second electrical representation to the output memory element coupled to the translator thereby enabling direct use of the output memory element with an information handling system utilizing the preselected format.

29. (NEW) The method of Claim 28 comprising the additional step of checking in the translator a memory format of the output memory element for agreement with a preselected memory format and initializing the format of the output memory element in accordance with the preselected memory format whenever said agreement is not found.

30. (NEW) A process for storing a digitized image in a camera comprising:

formatting the image into a digital image data file containing therein both image data and computer operation code, and

storing the digital image data file in a digital memory in the camera.

31. (NEW) The method of claim 30 further comprising:

compressing the digital image prior to the formatting step.

32. (NEW) For use in a camera having a digital memory and a plurality of user selectable modes of operation, a method for storing a digital image, comprising:

determining the user selected mode of operation;

generating a mode code corresponding to the user selected mode of operation;

compressing the digital image;

formatting the compressed digital image into a digital data file comprising the mode code, image data and computer operation code; and

storing the digital data file in the digital memory.

33. (NEW) For use in a camera having a digital memory, a plurality of user selectable image resolutions, and a switch allowing a user to select from a plurality of modes of operation, a method for storing a digital image, comprising:

determining from the status of the switch the mode of operation selected by the user;

generating a mode code corresponding to the mode of operation selected by the user;

determining the image resolution selected by the user;

generating a resolution code corresponding to the image resolution selected by the user;

compressing the digital image in accordance with the image resolution selected by the user;

formatting the digital image into a digital data file comprising image data and computer operation code;

writing the mode code into the digital data file;

writing the resolution code into the digital data file; and

storing the digital data file into the digital memory.

34. (NEW) For use in a digital camera having a digital memory, a plurality of user selectable image resolutions, a switch allowing a user to select from a plurality of modes of operation, and an image memory removably affixable thereto and having stored therein a plurality of digital image files each corresponding to the digital image, a method for storing a digital image, comprising:

determining from the status of the switch the mode of operation selected by the user;

generating a mode code corresponding to the mode of operation selected by the user;

determining the image resolution selected by the user;

generating a resolution code corresponding to the resolution selected by the user;

compressing the digital image in accordance with the resolution selected by the user;

formatting the digital image into a digital file comprising image data and computer operation code;

writing the mode code into the digital data file;

writing the resolution code into the digital data file;

storing the digital data file into the digital memory; and

transferring the digital data file from the digital memory to the image memory.

35. (NEW) An electronic camera operative to generate output data for use with a plurality of user selectable information handling systems, comprising:

a digitizer for generating digital data corresponding to a captured image;

a memory element for storing the digital data; and

an output controller for determining the selected information handling system and assigning a corresponding output data format code to the stored digital data.

36. (NEW) The camera of claim 35 further comprising:

a compression processor for compressing the digital image data prior to formatting in the digital control unit.

## REMARKS

With this Preliminary Amendment, new Claims 21-36, which respectively correspond to Claims 62-65, 72-74, 80-81 and 105-111 of the parent case, are presented herewith for examination.

Respectfully submitted,

Marc K. Roberts et al.

Date: April 3, 2000 By: _____

Gordon K. Harris, Jr.
Reg. No. 28,615
Attorney for Applicants

Harness, Dickey & Pierce, P.L.C.
P.O. Box 828
Bloomfield Hills, MI 48303
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# ELECTRONIC STILL VIDEO CAMERA WITH DIRECT PERSONAL COMPUTER (PC) COMPATIBLE DIGITAL FORMAT OUTPUT

## BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention generally relates to an electronic still video camera and in particular to an improved electronic still camera which converts a still picture of an object or scene into an operator selectable compressed digital signal format for storage utilizing a compression/decompression algorithm, such as the Joint Photographic Experts Group (JPEG) algorithm standard for example, formatted into Personal Computer (PC) compatible format retaining the images' color information, and stored on a PC compatible memory diskette. For example, the diskette can be a three and a half (3 1/2) inch digital diskette. The digital diskette is removeable from the electronic camera for direct insertion into a PC which contains the previously loaded corresponding decompression algorithm whereby the digital image is in a format compatible for immediate use with word processing, desk top publishing, data base, and multi-media applications.

2. Description of the Prior Art

Fig.1 is a schematic block diagram showing structure of a conventional prior art electronic still camera system, in which a CCD image sensor element 1a converts a still image of an object into an analog color video signal when the shutter control circuitry 2a is activated. The output color video signal of the image sensor element is then routed to the signal processing subsystem 3a where the signal is converted to National Television System Committee (NTSC) or other composite video formats (such as the European video standard Phase Alternating Line-PAL) and logged in analog format onto a mass memory storage device such as an analog video floppy disk, Electrically Erasable Programmable Read Only Memory (EEPROM), analog audio cassette, bubble memory, or other storage device 5a. Power is supplied by a rechargeable / removeable battery system 4a.

An electronic camera that converts an image into electronic image signals and transferred to a memory storage device is disclosed in the following: U.S. Patent No. 4,131,919; U.S. Patent No. 4,456,931; U.S. Patent No. 4,758,883; U.S. Patent No. 4,803,554; and U.S. Patent No. 4,837, 628.

Conventional prior art electronic still cameras, for example of the types disclosed in the aforementioned references, produce an electronic signal corresponding to a desired image in analog format such as the National Television System Committee (NTSC) or similar on magnetic or electronic storage media for either permanent or temporary storage to facilitate viewing on a television or video monitor. With the current state of the art, it is expensive and time consuming to

convert the analog image equivalent to a digital format for direct utilization with PC software applications. Currently, to convert an image captured on an electronic still camera to a PC compatible format one must convert the signal back to either a composite NTSC or RGB video signal and use a conversion device such as a "frame grabber" (a digital circuit board installed into PCs that convert video images into PC compatible formats) of the type sold commercially by Aapps Corporation, Orange Micro, RasterOps, and others or convert the image to a hard-copy print (a photograph) and utilize an electronic "scanner", a piece of equipment that connects to a PC, which converts an image into a digital format. The later technique is employed extensively within the desktop publishing industry.

## SUMMARY OF THE INVENTION

It is the object of this invention to provide an improved electronic still camera with operator selectable picture compression in one of a plurality of operator selectable digital data formats recordable on a standard removeable magnetic diskette common to personal computers.

It is a further object of this invention to provide an improved electronic still camera that provides digital image files for immediate and direct incorporation into popular word processing, desktop publishing, and other software programs on PCs.

It is another object of this invention is to provide an improved electronic still camera that, under user selection, can record and store still images selectively compressed in a directly insertable digital memory storage device into a PC in either color or black and white formats thus facilitating storage of a large number of images with the signal flag indicating the degree of compression selected by the operator as well as the color/black and white mode selection being stored as digital values on the digital memory storage device with each image frame.

An additional object of this invention to provide an electronic still camera device that can rapidly capture a series of images automatically as well as singularly. Also, this camera provides multiple outputs in both video format for monitor and display of images and digital formats to facilitate data transmission, additional processing, or storage to a variety of storage media.

It is still another object of this invention is to provide a more efficient electronic still camera that can take a still picture with operator selectable high, medium, or low resolution in either color or black and white by electronic shutter and exposure control by utilizing a variety of electro-optical sensors including Charge Coupled Devices (CCD), Infrared (IR), and Ultra Violet (UV) which can be directly or remotely controlled by analog, digital, or radio frequency (RF) control signals.

A further object of this invention is to provide a programmable video picture translator device for efficiently converting electronic still images in analog composite video format into digital data format readable by a PC. This translator device also provides additional video inputs and outputs for capturing video images, monitoring video images on monitors and displays, and can transmit either compressed or unprocessed digital image data through a variety of output I/O channels in various formats such as serial, parallel, etc. Also, this invention can incorporate sound/voice with images thru additional interface circuitry and audio digitizers.

Finally, it is the object of this invention to provide an electronic still camera that is efficient in design and permits extended periods of portable operation and which provides the user with operational status through the use of continuous internal self-test software routines and operator displays.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic block diagram of a conventional prior art electronic still camera .

FIG. 2 is a schematic block diagram of the of the overall structure of an electronic still camera embodying the present invention.

FIG. 2A is an illustration showing one embodiment of an audio data file, data format flag, compression level, and color/black and white mode selection values stored on a digital memory diskette storage device.

FIG. 3 is a flowchart showing the power-up and continuous self-test sequence in accordance with one aspect of the present invention.

FIG. 4 is an example of a 1/2" CCD array utilizable in accordance with one aspect of the present invention.

FIG. 5A is a schematic block diagram showing the image signal to digital signal conversion logic in accordance with one aspect of the present invention.

FIG. 5B is a logic and timing diagram for the image signal to digital signal conversion logic in accordance with one aspect of the present invention.

FIG. 6 is an example of the control panel logic in accordance with one aspect of the present invention.

FIG. 6A is an example of one embodiment of switch logic of the control panel switches and controls utilizable in accordance with one aspect of the present invention.

FIG. 6B is an example of the PICT image file format based upon the published standard provided by Apple Computer, Inc.

FIG. 6C is an alternate embodiment of the current invention embodying remote operation.

FIG. 7 is a simplified block diagram of the digital control unit in accordance with one aspect of the present invention.

FIG. 8 is a flowchart showing the steps of the image compression algorithm in accordance with one aspect of the present invention.

FIG. 9 is a block diagram of a video format translator device in accordance with one aspect of the present invention.

FIG.10 is a block diagram illustrating the operation of a translator device in accordance with one aspect of the present invention.

FIG.11 is an alternative embodiment of the video format translator in accordance with another aspect of the present invention showing additional video inputs and data outputs.

FIG.12 is an alternate embodiment of the invention showing an optional diskette format utility flowchart.

FIG.13 is an alternate embodiment of a frame buffer utilizable in accordance with another aspect of the present invention showing a frame buffer stack permitting multiple shot mode.

FIG. 14A is a block diagram of an embodiment of the format select logic in accordance with one aspect of the present invention.

FIG. 14B is a flow diagram illustrating the steps of the format selection logic operations

## DESCRIPTION OF THE PREFERRED EMBODIMENT

FIG. 2 is a schematic block diagram of the preferred embodiment of an electronic still camera in accordance with the principals of the invention. Referring to FIG. 2, an image optical pick-up element **1**, which for example could be a Charge Coupled Device (CCD) (or an Infrared (IR) or Ultraviolet (UV) sensor), converts a still image of an object into an electric signal when a picture "shoot" command is initiated by the operator via control panel **2**. When taking a picture, focusing and shutter speed are controlled by a lens system and shutter speed selection mechanism under control of the digital control unit **9**. The camera, like other still video cameras, employs an electronic shutter system that controls a charge storage time in a CCD array onto which an image of an object is focused through the lens system.

When the "shoot" control **6** is half depressed (see FIG. 6), a power supply voltage is supplied from the rechargeable batteries **4** to the electronic circuits and digital control unit **9**, control panel **2**, and the disk drive assembly **5**. The exposure control circuitry not shown generates appropriate horizontal and vertical transfer pulses as well as field shift pulses under control of the reference clock timing and control signals provided by the digital control unit **9** type for driving the CCD

device and pre-processing circuitry. This design may be of any type well known in the art for example those cited in Patents 4,131,919 and 4,456,931 and any similar designs well known in the prior art.

An alternate embodiment of the present invention that provides remote operation of the camera is shown in FIG. 6C. When remote "Shoot" control **30** is activated by any means for example manually, or by radiant, or electronic energy, a control signal is generated and routed through the external jack **31**, located on the external camera body. The external control **30** is electrically connected to the external jack **31** by a twisted-pair conductive cable assembly that is familiar to those skilled in the art. Upon receipt of the externally generated "shoot" command, the relay switch **32** is activated and provides internal switch closure. This closure of switch **32** then initiates the process previously described and provides the half V+ voltage previously described. The full V+ is provided via the fixed delay **33**, the value chosen to allow the diskette drive assembly **5** (FIG.2) and associated control circuitry to initialize prior to receiving image data.

When the "shoot" control is fully depressed in either embodiment, the shutter controller **15** (FIG. 6) generates a shutter pulse that generates control signals for the A/D converters **8** allowing the image/picture data signal in the sample and hold circuitry of the pixel multiplexer **7** to be converted into a digital signal. Control and address instructions of the type well known in the art are generated from the digital control unit **9** to facilitate the storage of the digital image data within the pixel buffer **10** and frame buffer **11**. Upon completion of image conversion, the contents of the frame buffer are transferred to the compression processor **12** which for example may be of the many versions currently offered commercially such as C-Cube's (San Jose, California) four chip Application Specific Integrated Circuit (ASIC) set. In the compression processor **12**, the Joint Photographic Experts Group (JPEG), a part of the International Standards Organization (ISO) which is a subset of the International Telegraph and Telephone Committee (CCITT), image compression algorithm fully described in Report # JTC1/SC2/WG8 dated 1985 is performed under control of the digital control unit **9** to compress the size of the image. A variable selectable compression ratio of up to 50:1 is performed on the digital image frame. Other compression ratios are operator selectable via the control panel **2** switches **14A** and **14B** (FIG. 6). The compressed digital frame is then formatted into either an IBM PC/Clone (such as GIFF) or Apple Macintosh (such as PICT II) image file format depending on the setting selected by the operator for a user switch **17** (FIG. 6) position on the control panel **2**. After formatting, the file is written into a temporary memory buffer within the disk input/output (I/O) interface circuit **13** which, under the command of

the digital control unit 9, controls the high density (1.4 Mbyte storage capacity) disk drive unit 5. Following file transfer to the diskette e.g., the frame counter display 22 on the control panel 2 is updated by appropriate control signals and the camera is ready to undergo the same procedure for the next image. Power to the electronic circuits and disk drive system is terminated following release of the "shoot" control switch 6.

In accordance with the preferred embodiment of this invention, it is permissible for the user to select various resolution quality image recording levels with the higher levels being at the expense of memory diskette storage capacity. The position of switches **14A** and **14B** for example could represent a unique digital mark or word that denotes the respective switch position and is sensed during initial power application and periodically during operation. FIG. 6A illustrates typical logic AND gate circuits **60a** and **60b** utilizable in conjunction with switches **14A** and **14B** or switch **17** to generate appropriate signals to designate respective switch positions and generate appropriate control signals from. The switch positioned in the High position for high resolution allows only four to five images to be stored, while Med. switch position for medium resolution allows approximately twenty five images to be stored, and Low for low resolution allows up to fifty images to be stored on a single diskette. Also, by selecting black and white mode instead of color via switch **14B**, the operator may select additional storage capacity since storage is increased by a factor greater than three (one element per pixel versus three for color). Various image resolution combinations are permissible because the operator can select a different resolution and mode setting for each image prior to image signal capture. This is accomplished by marking or "tagging" each image frame data information signal with the resolution and mode of each image as it is written onto the memory diskette in any suitable manner, for example as shown in FIG 2A. With reference to FIG 2A, diskette **50** has tracks **51a, 52b, ....52n**. With reference to track **52b** there is shown a representative portion of segment **53** depicting a typical image file information format having digital bit **54** depicting color mode, and digital bits **55** representing compression resolution level markings or tags. With reference to color mode tag **54** it can be seen that if switch **14B** is in the color position tag **54** is recorded as a logical "one" or true-conversely if bit **54** is recorded as a logical "zero" it corresponds to the black and white position of switch **14B**. Similarly as shown switch **14A** would record in memory position **55** a binary "zero" for low resolution, a binary "one" for medium resolution and a binary "two" for high resolution selections by the operator. By incorporating this "tagging" approach, it is possible for the decompression algorithm, loaded into any PC prior to use or written onto the memory storage

diskette along with the image data, to automatically determine the appropriate level of compression associated with image file and execute decompression efficiently.

Still another alternate embodiment in accordance with this invention incorporates an acoustic digitizer circuit which digitizes sound. There are several digitizers commercially available such as the Apple Computer Inc. Musical Instrument Data Interface (MIDI) adaptor. The output of this digitizer may be selectively connected to the CPU **20** (FIG 7) via an additional I/O interface similar to the auxiliary I/O interface **80**. The sound or audio associated with each image can be recorded, digitized, and stored on the diskette device on available tracks in an identical manner previously described (FIG 2A). An image file in accordance with this embodiment would be appropriately marked or tagged with the corresponding digitized audio file **56** (FIG 2A). Upon playback on a sound configured PC, both the image and the corresponding audio would then be viewed and heard simultaneously.

It should be noted that a major advantage a camera in accordance with the present invention has over conventional still video cameras is that a camera according to this invention is capable of storing multiple digital images in semiconductor memory temporarily at a rapid rate while, simultaneously, the image compression processor **12**, file formatter software algorithm, and disk I/O interface **13** that stores formatted files continue to function in concert together at a slower rate. This efficient design coupled with VLSI low power, high speed semiconductor memory devices (**10** & **11** FIG. 5A and **24** FIG. 7) allows this operational capability.

Like most other still video and conventional film cameras, when the "shoot" control **6** (FIG. 6) is fully depressed, a control signal is generated from the digital control unit **9** that generates a trigger signal on the control panel **2** to cause a flash unit **16** (FIG. 6) to irradiate a flash of light onto the subject image.

During initial camera operation, the user first inserts a diskette such as a standard three and a half inch or similar storage medium. Various memory diskette sizes and formats are suitable for the invention. However, for the preferred embodiment either a double-density (800 Kbytes of storage) or a high-density (1.4 Mbytes of storage) diskette in a three and a half inch format which are readily available from various commercial sources such as Sony, Maxell, and Verbatim. The user must then select the desired PC format (IBM PC/Clone or Apple Macintosh, etc.) via switch **17** (FIG. 6) on the control panel **2**. As shown in FIG. 3.; after turning on the power switch or inserting a diskette **50**, the digital control unit **9** performs a self test of all internal circuitry, battery, disk drive unit, and control panel. Should any failures be detected, an appropriate error indicator is

illuminated on the control panel. During the power-on sequence (see FIG. 3 and FIG. 12), the inserted diskette **50** is automatically checked for formatting consistencies in accordance with the format selected by the format switch **17** on the control panel **2** (IBM/Apple/etc.) and for available storage space by checking the boot block on the diskette, a technique that will be familiar to those skilled in the art. Should any inconsistencies be detected, an error indicator is illuminated on the control panel (ie, disk full, unformatted, etc.). The operator frame counter display **22** (FIG. 6) is then updated to show the maximum number of pictures available based upon indicated operator selections (color/black and white), diskette type (double versus high density), and capacity (partially full versus empty diskette). During operation, the operator can selectively erase a frame and record over it if desired by selecting the erase mode of operation from the control panel and toggling the forward/reverse control.

The optics for the preferred embodiment of the invention is a commercially available one-half inch (1/2") color CCD device having a pixel grid array of 780 x 488 as pictorially depicted in FIG. 4. This results in 380,640 pixel elements which results in a commercially acceptable quality resolution image as will be understood by those skilled in the art. In a color imaging device (CCD array) photoelectric elements, such as photodiodes, are arranged in a two dimensional array with optical filters for R (red), G (green), and B (blue). Various arrangements of optical filters are well known and the arrangement of optical filters is not limited to a particular one with this invention. During operation each pixel stores a charge corresponding to the amount of incident light. The RGB components of each pixel's charge is sequentially read out via a horizontal / vertical addressing scheme that will be familiar to those skilled in the art.

As shown in FIG. 5A; each charge, when addressed, is amplified and processed in a sample and hold (S/H) circuit **18**. The analog voltage in each S/H circuit is digitized by an associated analog to digital (A/D) converter **8**. The digital values are routed and collected in the pixel buffer **10**. Following completion of discrete pixel element conversion and subsequent formatting in the pixel buffer which is under Control Processor Unit (CPU) **20** software control, the output of the full pixel buffer is routed to the frame buffer **11** by digital control unit **9**. This process continues until a complete frame is collected within the frame buffer.The general digital logic and timing and control signals for this circuitry is shown in FIG 5B.The timing is provided by a master clock that is an integral part of the CPU microprocessor. For example, the MOTOROLA 68040 microprocessor has a clock speed of approximately 40 Megahertz (MHZ) which results in a clock period of 25 nanoseconds (nsec.). This clock pulse is used by the function and address decoder

19 (FIG. 6) to generate the address and control signals shown in FIG 5B as would be understood by those skilled in the art. The circuit of the present invention may be designed by one skilled in the art to function with a variety of microprocessor architectures and is not limited to any one in particular. One can see from the timing chart that the S/H circuit is allowed (via the SE command) to charge to a voltage level indicative of the analog voltage impinging upon the pixel element (via the PS command). After a fixed time period, the A/D converters are enabled(via the CE command) to begin conversion of the analog voltage value on the S/H. Upon completion of conversion, a conversion completion signal (CC) is generated by the A/D and routed back to the S/H circuit (via the SC command which is generated by the function and address controller 19) to discharge the stored analog voltage in anticipation of the next pixel element conversion process. Next, the output of the A/D converter 8 is clocked into the pixel buffer 10 (via the PB command). When the pixel buffer 10 is full, the output is clocked out to the frame buffer 11 (via the FB command) and the pixel multiplexer address circuitry selects the next pixel for conversion. Reset signals (RST) are sent to all circuit elements to allow these devices to reset prior to receiving the next analog value.

Another novel concept of the present invention as illustrated in FIG. 5A and 5B utilizes a technique of paralleling the S/H and A/D devices for each pixel element thus accelerating the image signal analog-to-digital conversion process. This is accomplished by eliminating the serial S/H and A/D path typical of prior art still video camera designs. In addition, high-speed, low-power devices available from Sony, Burr-Brown, Datel, Analog Devices, and others facilitate the increased conversion throughput of the S/H and A/D circuits with pixel conversion times of less than 150 nanoseconds (nsec.). For example, Sony's video A/D converter Device part number CXA1016P/K performs up to 50 million samples per second or 20 nsec. per conversion. This device, or similar, may be used in the preferred embodiment of the present invention. As explained previously, prior art still video camera designs multiplex each signal component into a common/singular A/D path to reduce the number of components and power consumption. However, in accordance with another aspect of the present invention components such as C-MOS and ECL devices coupled with miniaturized packaging techniques such as surface mount devices (SMD) and ASIC technology make it feasible to incorporate these devices in a parallel design in order to realize a substantial increase in conversion speed with no appreciable increase in power consumption. Therefore, this design approach provides significant conversion throughput increases over previous designs.

The extremely high conversion speed in accordance with another concept of the present invention makes multiple high-speed camera operation possible in an alternate embodiment. For example, total conversion time required for the aforementioned CCD array utilizing the circuit of the present invention (FIG 5A) requires approximately 380,640 x 150 nsec. or 38 milliseconds (msec.). Additional time (approximately 5 msec.) is required for timing and control signal latency. Thus, total conversion time for a complete image frame prior to compression processing and logging to the memory storage diskette **50** is less than fifty msec. This allows for approximately 20 images to be captured in a one second period. By adding additional RAM **11A** (FIG.13) or other forms of commercially available random access memory to the frame buffer **11**, image frames could be "pushed" onto a semiconductor memory stack for temporary storage allowing the compression processor and data interface circuitry to perform their respective functions at a slower rate. As shown in FIG 13, each unprocessed image frame would be recorded or "pulled" from the stack on a "First-In, First-Out" (FIFO) manner until all images in the stack queue were processed and written to the storage diskette via the disk I/O circuitry **13**.

As shown in FIG. 6, control panel settings are monitored by the CPU **20**, a microprocessor, thus allowing the appropriate timing, control, and signal processing to be effected properly. The microprocessor **20** may be of the type 68040 manufactured by MOTOROLA, Intel's 80386 series, or equivalent microprocessors which specifications are commercially available and are incorporated herein by reference. The microprocessor utilization of this invention, which is in the digital control unit **9**, transmits commands and status to specific controls, functions, and displays in the control panel as well as receiving both circuit status/control data and operator commands through polling the operator switch settings **14A**, **14B**, and **17** via the bidirectional function and address decoder **19**. This approach allows the user to know immediately how much storage capacity remains in the image storage diskette **50** as well as the camera's overall operational and functional status through the use of status displays **21**, **22**, and **23** and ongoing software self-tests running in the background as depicted in FIG. 3. An example of this would be a low battery situation. First, the digital control unit **9** would detect a failure in the self-test mode. Next, the self-test light emitting diode **21** (FIG. 6) would be illuminated and an appropriate error display would be illuminated in the status display **22** thus providing the user with an exact indication of the error. Another example illustrating the operation of this embedded microprocessor type of control approach is the format switch **17** (FIG.6). The position of the format switch **17** is sensed upon power application. Following

diskette insertion, the boot block on the diskette is compared with the format switch **17** setting (IBM/clone or Apple) and if the format does not match or if the disk **50** is unformatted, the disk format status light emitting diode **23** would be illuminated and an appropriate error display would be illuminated in the status display **22** thus prompting the user to take appropriate corrective measures.

An alternate embodiment of the present invention involves adding an auxiliary I/O interface circuit or port to the digital control unit **9**. As shown if FIG.7, the auxiliary I/O port **80** connects in a manner similar to the Disk I/O interface **13**.This additional I/O channel provides for external control and monitor of all timing and control signals internal to the camera. In addition, it allows for the image data to be routed past or around the compression processor out to any additional internal or external device such as an optical disk storage device, digital analyzer, or other data processors that might be desired.

FIG. 7 shows the digital control unit **9**. The microprocessor **20** architecture here is typical to one familiar with the art. The frame buffer **11** (FIG.5A) receives and stores the outputs of the pixel buffer **10** until a complete frame of image data is received. Then, the CPU **20**, under software control, issues a control signal to the optics logic in the shutter and control circuitry **15** (FIG.6) thus resetting those functions for future image recording. The full frame buffer **11**, upon command from the CPU **20**, transfers it's data into the compression processor **12** (FIG. 2) which performs thousands of levels of parallel pipeline processing on the image data. The compressed image frame is then written out to the mass memory RAM (Random Access Memory) **24** where it is temporarily stored until transferred to the disk drive assembly **5** via the disk I/O interface circuitry **13**.

Referring to FIG. 8, a flowchart shows the steps involved in the image compression process performed by the image compression processor **12** (FIG.2) in accordance with the preferred embodiment of the present invention. The output of the frame buffer **11** is transferred into the input of the image compression processor **12** under the control of the digital control unit **9**. As previously described, the setting of switch **14A** (FIG 6) is read by the CPU **20** (FIG. 7) to determine the image resolution quality desired. Depending on the operator selected setting of switch **14A**, the unique digital word generated by the AND gate **60a-b** (FIG.6A) which is activated by the selected position of switch **14A** is routed to image compression processor **12** via CPU **20** (FIG. 7) which selects for example a predetermined digital memory location containing the appropriate corresponding compression ratio parameters under program control. The compression processor uses this command value for example to establish the size of the covariance matrix and a threshold for acceptance for the variances produced by the Discrete Cosine

Transformation (DCT) transform coefficients. Next, the digital image signals are converted from the RGB format previously discussed in connection with Figures 2, 5, and 6 into luminance and chrominance signals. The luminance and chrominance signals subsequently undergo a DCT. The cosine transformed signals are then quantized and are then processed for Huffman coding. The Huffman coded image signals are then formatted into a form that facilitates format processing into various PC compatible formats (GIFF, PICT2, etc.). For a more complete understanding of the image compression process reference may be made to I.E.E.E. Catalog No. EH0231-1, Library of Congress No. 85-60384 published by the I.E.E.E. Society dated 1985 and incorporated herein by reference.

Of the two traditional classes of image compression techniques, spatial coding and transform coding, transform coding techniques lend themselves well for this application due to computational simplicity. Transform coding techniques that provide good visual fidelity include: Karhunen-Loeve transform (KLT), Fourier, cosine, sine, and Hadamard. The KLT algorithm offers the best visual fidelity but suffers from serious computational complications due to extremely large matrix size. Several alternate algorithms that offer reasonable visual fidelity that are computationally feasible for this invention include the Fast Fourier Transform (FFT), Discrete Cosine Transform (DCT), and Discrete Sine Transform (DST). The DCT was adopted by the JPEG as the preferred algorithm due to computational simplicity and performance.

It should be noted that the Joint Photographic Experts Group (JPEG) ( composed of experts from many companies including IBM, AT&T, Digital Equipment Corp, and INTEL) compression/decompression standard was developed in 1985 in response to the lack of interoperability between image and processing equipment due to numerous proprietary standards held by each manufacturer. The JPEG standard provides image compression effectively up to 75 times or greater depending on the visual fidelity desired. The JPEG standard is widely used in industry as an alternative to proprietary algorithms such as Intel's own proprietary standard called DVI which was initially developed by RCA before being sold to INTEL, the integrated Circuit manufacturer. INTEL offers it's own firmware compression processor incorporating their DVI standard delivering compression ratios in excessive of 100:1. However, a new international standard called MPEG is due to be announced in the 1991 time frame from the JPEG and should offer compression ratios of 275:1 and greater. In the preferred embodiment of the present invention, the JPEG standard is the preferred algorithm chosen with the incorporation of the the MPEG standard or other similar standard in the future when available commercially. An alternate embodiment of the present invention would be

the incorporation of various proprietary compression algorithm standards such as DVI.

The compression/decompression algorithm firmware implementation of the JPEG algorithm is available commercially from various sources including C-Cube, Electronics for Imaging, Storm Technology, Burr-Brown, Spectral Innovations Inc., INTEL, and others. The implementation of this algorithm for the present invention may incorporate the integrated circuit set commercially available from C-Cube. Their four chip ASIC JPEG algorithm implementation is performed in three basic steps: first, the image is divided into 8-by-8 pixel squares and applies a discrete cosine transform (DCT) to each square resulting in 64 frequency values; second, these frequencies are put through a quantization algorithm to eliminate unimportant frequencies; third, the remaining values are run through a Huffman coding scheme to encode the most frequently occurring values using the fewest bits. A compatible software implementation of the JPEG algorithm is available commercially from Aladdin Systems, Radius Inc., Kodak, and others.

Those skilled in the art will be familiar with the process and the commercially available software and firmware chipsets that are currently available on the market. The present invention incorporates both available firmware chipsets in the camera and software for use in the PC for decompression. The decompression algorithm can be written onto the camera's diskette **50** prior to any image data recording. This allows the PC user to take the diskette **50** to a PC and directly incorporate the image data because the image file selected by the user is automatically decompressed transparent to the user. The algorithm can be written onto an unused track **52** or sector combination on the diskette as shown on FIG 2A. Alternatively, the decompression algorithm can be loaded onto a PC before inserting a diskette **50** containing compressed image data. In the latter embodiment the resolution and mode values **54** and **55** (FIG 2A.) for each representative image would be read from diskette **50** in order to appropriately control the selection and activation of the appropriate corresponding decompression algorithm.

As shown in FIG.7, the output of the image compression processor **12** is routed to the RAM memory **24** where the compressed image is formatted for either the PICT II or GIFF format depending on the setting of format switch **17** (FIG. 6). It should be noted that a large number of image formats for PCs exist. PICT and GIFF are the most common for the Apple and IBM PC's and are therefore the preferred formats for the present invention although other formats can be easily incorporated into the design by changing the software format routines. These software image formats are commercially available from many sources most notably Apple computers for PICT and IBM for GIFF. An example of the PICT format is

pictorially shown in FIG. 6B as will be familiar to those skilled in the computer arts. Once formatting is complete, the formatted image data is transferred to the disk I/O interface **13** for transfer to the magnetic recording diskette **50**.

FIG. 9 and FIG. 10 illustrate the preferred embodiment of the video format translator device in accordance with another aspect of this invention that converts other still video camera formats for example on two inch video diskette to this invention's selectable PC compatible digital format. The general concept of operation is shown in FIG. 10. In FIG. 9 correspond parts and subassemblies in translator **40** are shown with like numbers corresponding to FIG. 2 and 6 having a **40** hyphenation prefix designation and such parts and subassemblies perform similar functions to those described above with reference to FIG.s 2 and 6. Referring again to FIG. 9, the translator **40** incorporates the same components utilized in the digital circuit card assembly which houses both the digital control unit **9** and optics processing circuits (pixel multiplexer **7**, A/D **8**, etc. **10-13**). The major difference is that the CCD array **1** is replaced with an input disk drive **25**, for example a two inch (2") video disk drive assembly, and an NTSC video format decoder **26** which converts the composite video signal to an RGB format for processing as described previously.

FIG 11. displays an alternate embodiment of the video format translator device **40** of the present invention that shows optional inputs **27** and outputs **28** and **29**. The exact same circuitry is utilized that was used for the translator device **40** as shown in FIG. 9 except that inputs **27** for either an NTSC/PAL format or RGB format video signal is provided. This allows video signals from other sources such as a cable TV, CAMCORDER, or other video signal source to be digitized and archived in a PC compatible format. Also, provisions for video output jacks **28** are made to allow either viewing of the image / video source prior to or during image recording. Finally, provisions are made to provide a data output **29** to allow connection to other PC peripherals such as a communications modem, larger/smaller disk drive assembly, optical disk, specialty display or signal processor / analyzer. Either a standard serial, parallel, or Small Computer Standard Interface (SCSI) data port can be readily connected to the auxiliary I/O interface **80**.

FIG. 12 depicts an alternate feature of an embodiment of the present invention that shows how an inserted diskette **50** that is either unformatted or formatted for a undesired (e.g., not corresponding to the setting of switch **17**-FIG. 6) PC configuration would be automatically properly formatted for use with a camera in accordance with another aspect of this invention. This capability allows the user of this invention to forego the requirement to pre-format the storage medium (diskette) on a PC prior to using it in the camera operated in accordance

with the present invention. With reference to FIG.3 the power-on sequence process would result in an abnormal diskette format error if the format of an inserted diskette **50** did not correspond to the operator selected format switch **17** (FIG.6). In accordance with the automatic diskette format option, CPU **20** of digital control unit **9** in response to the abnormal diskette format error would initiate the diskette format process illustrated in FIG.12. Upon completion of the diskette format process illustrated in FIG.12, the power-on sequence illustrated in FIG.3 would continue from step B.

Referring now to FIG. 14A, there is shown a schematic block diagram of the format selection logic in accordance with another aspect of the present invention. During the power-on sequence as described in connection with Figures 3 and 12, processor **20** of control unit **9** initiates a format selection switch sample and test routine as more fully described in the flow diagram illustrated in FIG. 14B. Switch **17** is illustrated in FIG 14A in the Apple PC position and logic level v1 is applied as inputs to logic gates **60c** and **60d**. As illustrated in FIG. 2A, the format signals **57** for the Apple PC format is a logic "zero" and conversely the format signal or tag **57** if the format switch **17** were in the IBM PC or other computer type position would be a logic "one" and "two" respectively. In response to the logic "zero" indicating Apple PC format, processor **20** accesses a unique memory location **XY** of format memory **20-2** which for example may comprise any random access memory with two megabytes storage capacity. The data format for the operator selectable predetermined number of computer architectures, similar in content and arrangement to those illustrated in FIG. 6B for an Apple PC would be stored in memory **20-2** which would be addressed in response to the other operator selectable position of switch **17** to generate the other unique codes **57** as shown in FIG 2A. Processor **20** in response to a stored format subroutine more particularly shown in FIG. 14B contains the allocation of data memory addresses in disk input/output interface unit **13** in accordance with the picture image file format as illustrated in FIG. 6B. Thus the digital video data information signals generated by compression processor **12** are appropriately formatted and stored in memory storage disk drive **5** to insure compatibility with the format selected by the operator by selectively positioning switch **17.**

Those skilled in the art will recognize the many alterations, additions or changes of the preferred embodiment may be made without departing from the scope of the following claims.

What is claimed is:

Claim 1. In an electronic still image camera comprising:

an optical lens,

a shutter mechanism operably associated with said lens,

an array of discrete light sensing pixel elements, each pixel element being responsive when said shutter mechanism is operated to incident illumination from a subject image radiating through said lens and shutter mechanism to generate an analog picture information signal corresponding to said subject image,

pixel multiplexing means responsive to each array of pixel elements for separating an output from each pixel element into its primary color components,

analog to digital converter means responsive to the outputs of said pixel multiplexing means for converting said analog signals into corresponding digital data information signals,

digital data compression means for applying a digital data compression algorithm to said digital data information signals to generate compressed digital data information signals, and

removably mounted memory means for storing said compressed digital data information signals,

the improvement comprising operator selectable control means for controlling digital data format compatability between said compressed digital data information signals and one of a plurality of operator selectable types of computer apparatus.

Claim 2. The improved electronic still image camera of Claim 1 further comprising switch activated control means for improving the image signal storage efficiency by selectively determining the amount of storage of said removable memory means to be associated with storage of each picture image.

Claim 3. The improved electronic still camera of Claim 1 further comprising picture image resolution determining means for selectively determining which of a predetermined set of compression algorithm parameters are to be applied to said digital data information signals in response to an operator activated switch means.

Claim 4. The improved electronic still camera of Claim 3 further comprising record marking means for generating and recording with each said image digital data information signals a coded mark indicating the compression algorithm parameters utilized in compressing said image digital data information signals.

Claim 5. The improved electronic still image camera of Claim 1 wherein said removable memory means comprises digital data diskette means having thereon a plurality of selectively addressable magnetic sector and track sections for recording said compressed digital data information signals.

Claim 6. The improved electronic still image camera of Claim 1 further comprising memory formatting means operable during the camera power-up routine to automatically format said memory means in accordance with one of a plurality of operator selectable type of computer apparatus.

Claim 7. The improved electronic still image camera of Claim 5 wherein said digital data compression algorithm of said digital data compression means is also recorded in its entirety on said diskette means and further comprising record marking means for recording a digital coded mark for indicating the compression algorithm parameters utilized in compressing each said image digital data information signal.

Claim 8. The improved electronic still image camera of Claim 1 further comprising audio recording means for simultaneously recording audio signals associated with each subject image and memory file correlation means for associating in

said memory means the respective storage locations of said audio signals with its associated image signals.

Claim 9. The improved electronic still image camera of Claim 3 further comprising record marking means for recording a unique mark indicating the compression algorithm parameters utilized in compressing each said image digital data information signal.

Claim 10. An electronic still image camera comprising:

an optical lens,

a shutter mechanism operably associated with said lens,

an array of discrete light sensing pixel elements, each pixel element being responsive when said shutter mechanism is operated to incident illumination from a subject image radiating through said lens to generate an analog picture information signal corresponding to said subject image,

pixel multiplexing means responsive to said array of pixel elements for separating an output from each pixel element into its primary color components,

analog to digital converter means responsive to the outputs of said pixel multiplexing means for converting said analog signals into corresponding digital data information signals,

digital data compression means for applying a digital data compression algorithm to said digital data information signals to generate selectively compressed digital data information signals,

removably mounted memory means for temporarily storing said compressed digital data information signals,

and selectable control means for controlling digital data format compatability between said compressed digital data information signals and one of a plurality of predetermined selectable types of computer apparatus.

Claim 11. The electronic still image camera of Claim 10 further comprising memory formatting means operable to automatically format said data stored in memory means in accordance with one of a plurality of operator selectable data storage formats.

Claim 12. The electronic still image camera of Claim 10 further comprising image resolution determining means for selectively determining which of a predetermined set of compression algorithm parameters of said digital data compression means are to be applied to said digital data information signals.

Claim 13. The electronic still image camera of Claim 12 further comprising record marking means for marking each said image digital data information signal to indicate which one of said predetermined set of compression algorithm parameters were utilized to compress said image digital data information signals.

Claim 14. The electronic still image camera of Claim 10 wherein said removably mounted memory means comprises digital data diskette means and further comprising selectable diskette formatting for automatically formatting said diskette means in accordance with one of a plurality of operator selectable data format types.

Claim 15. A process for storing an electronically sensed video image of an electronic still image camera comprising the steps of:

Generating an analog signal corresponding to the radiant light incident on a predetermined number of light sensing pixel elements to generate analog image signals,

Converting the analog image signals into digital electronic information signals wherein a distinct digital electronic signal corresponds to the analog image signals corresponding to the intensity of radiant light falling on the light sensing pixel elements,

Temporarily storing the digital electronic information signals,

Compressing the digital electronic information signals by applying a data compression algorithm to sort digital electronic information signals,

Selecting one of a plurality of predetermined data formats corresponding to a like plurality of data formats of a like number of types of computer apparatus, and

Storing said compressed digital electronic information signals in said predetermined data format in a digital memory.

Claim 16. The process of Claim 15 further including the steps of:

Detecting the presence or occurance of one or more of a predetermined number of conditions, and

Selectively activating said generating of the analog signal in response to the detection of said condition.

Claim 17. The process of Claim 15 further including the steps of:

Recording audio signals which relate to said analog image signals, and

Storing said audio signals in operable conjunction with said digital information signals such that both the audio and image signals can be retrieved.

Claim 18. An electronic video still image camera data format translator comprising:

Input means for producing electronic analog image signals corresponding to the outputs of a plurality of light sensing pixel elements corresponding to a predetermined number of discrete image sensing elements.

Analog to digital converter means for converting said analog image signals into corresponding digital image signals corresponding to said array of such predetermined number of discrete image sensing elements.

Buffer means for storing image forms.

Compression selection means for applying a predetermined compression algorithm to said digital image signals.

Format selection means for determining one of a number of predetermined data formats in which said compressed digital image is to be stored and

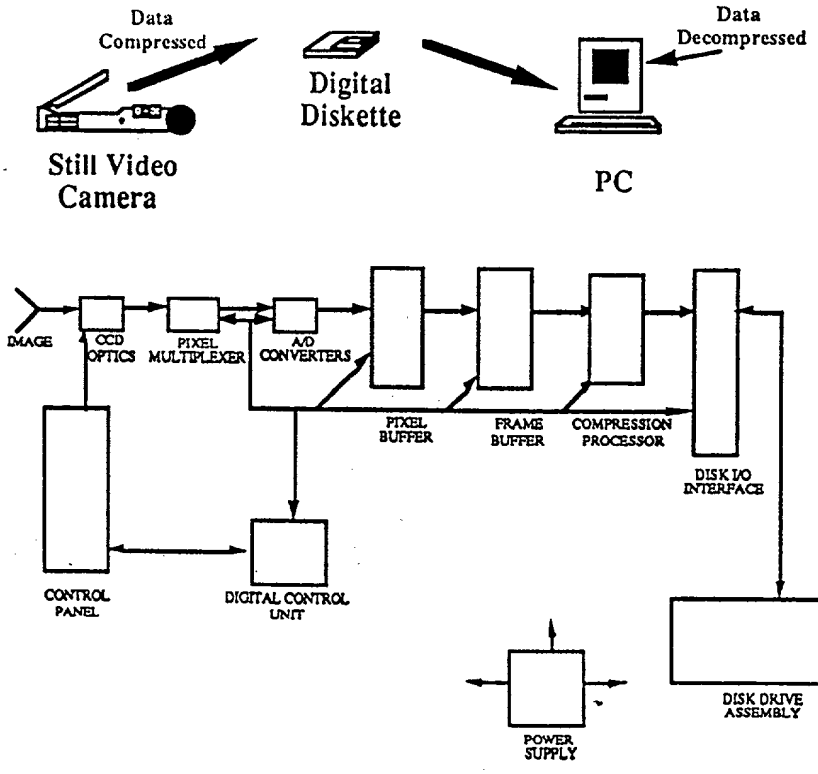
Removable memory means for storing said digital images in said predetermined data format.

Claim 19. The electronic still image camera of Claim 10 wherein said pixel multiplexing means further comprises parallel processing switching means for simultaneously parallel processing the output of each such pixel element.

Claim 20. The electronic still image camera of Claim 10 further comprising remote activation means for selectively activating said camera.

## ABSTRACT

An electronic still camera comprising a lens, shutter, and exposure control system, a focus and range control circuit, a solid state imaging device incorporating a Charge Coupled Device (CCD) through which an image is focused, a digital control unit through which timing and control of an image for electronic processing is accomplished, an Analog-to-Digital (A/D) converter circuit to convert the analog picture signals into their digital equivalents, a pixel buffer for collecting a complete row of an image's digital equivalent, a frame buffer for collecting all rows of an image's digital equivalent, and a selectively adjustable digital image compression and decompression algorithm that compresses the size of a digital image and selectively formats the compressed digital image to a compatible format for either the IBM Personal Computer and related architectures or the Apple Macintosh PC architecture as selected by the operator so that the digital image can be directly read into most word processing, desktop publishing, and data base software packages including means for executing the appropriate selected decompression algorithm; and a memory input/output interface that provides both temporary storage of the digital image and controls the transmission and interface with a standard Personal Computer (PC) memory storage device such as a digital diskette. The digital diskette is removably inserted into the housing of the camera prior to use in recording digital image data.

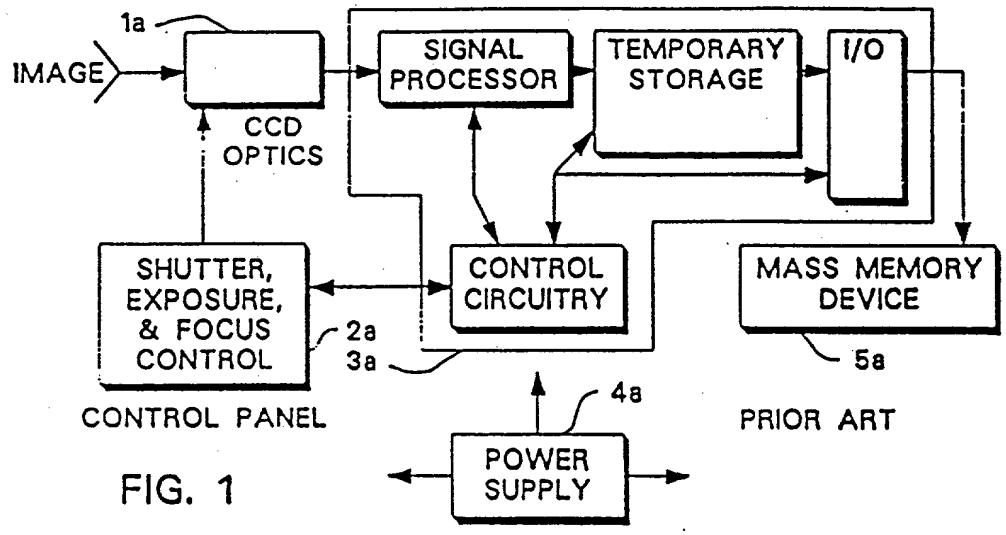

1a
IMAGE
CCD OPTICS
SIGNAL PROCESSOR
TEMPORARY STORAGE
I/O
SHUTTER, EXPOSURE, & FOCUS CONTROL
2a
3a
CONTROL CIRCUITRY
MASS MEMORY DEVICE
5a
CONTROL PANEL
4a
POWER SUPPLY
PRIOR ART

FIG. 1

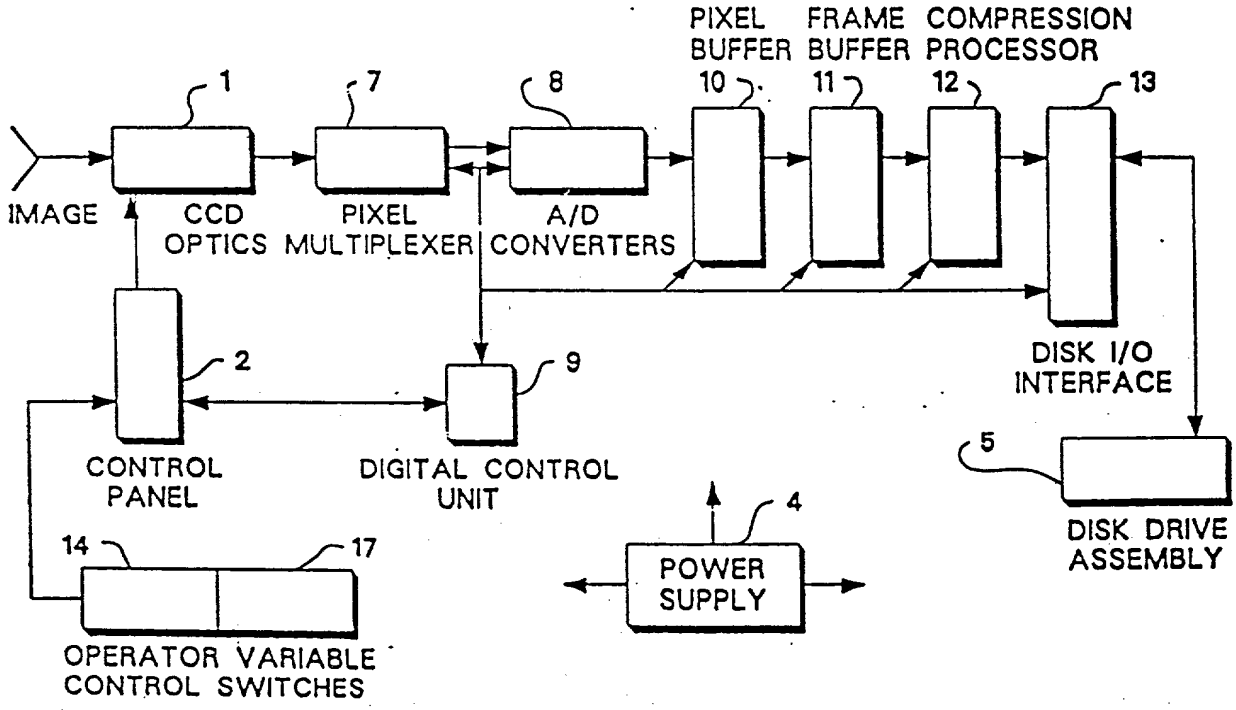

PIXEL BUFFER
FRAME BUFFER
COMPRESSION PROCESSOR
1
7
8
10
11
12
13
IMAGE
CCD OPTICS
PIXEL MULTIPLEXER
A/D CONVERTERS
2
9
DISK I/O INTERFACE
CONTROL PANEL
DIGITAL CONTROL UNIT
5
DISK DRIVE ASSEMBLY
4
POWER SUPPLY
14
17
OPERATOR VARIABLE CONTROL SWITCHES

FIG. 2

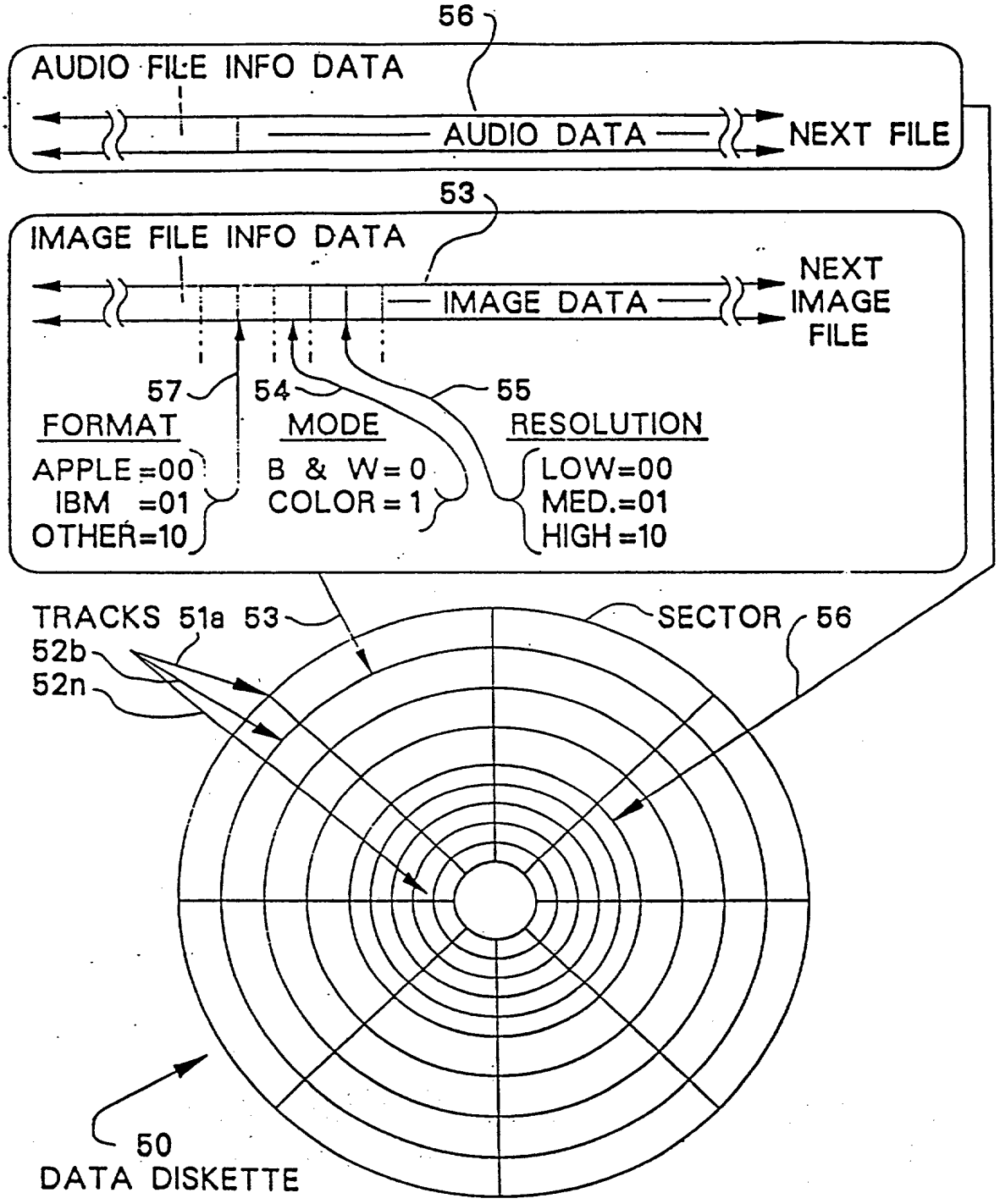

56
AUDIO FILE INFO DATA
AUDIO DATA
NEXT FILE
53
IMAGE FILE INFO DATA
IMAGE DATA
NEXT IMAGE FILE
57
54
55
FORMAT
APPLE=00
IBM =01
OTHER=10
MODE
B & W=0
COLOR=1
RESOLUTION
LOW=00
MED.=01
HIGH=10
TRACKS 51a
52b
52n
53
SECTOR
56
50
DATA DISKETTE

FIG. 2A

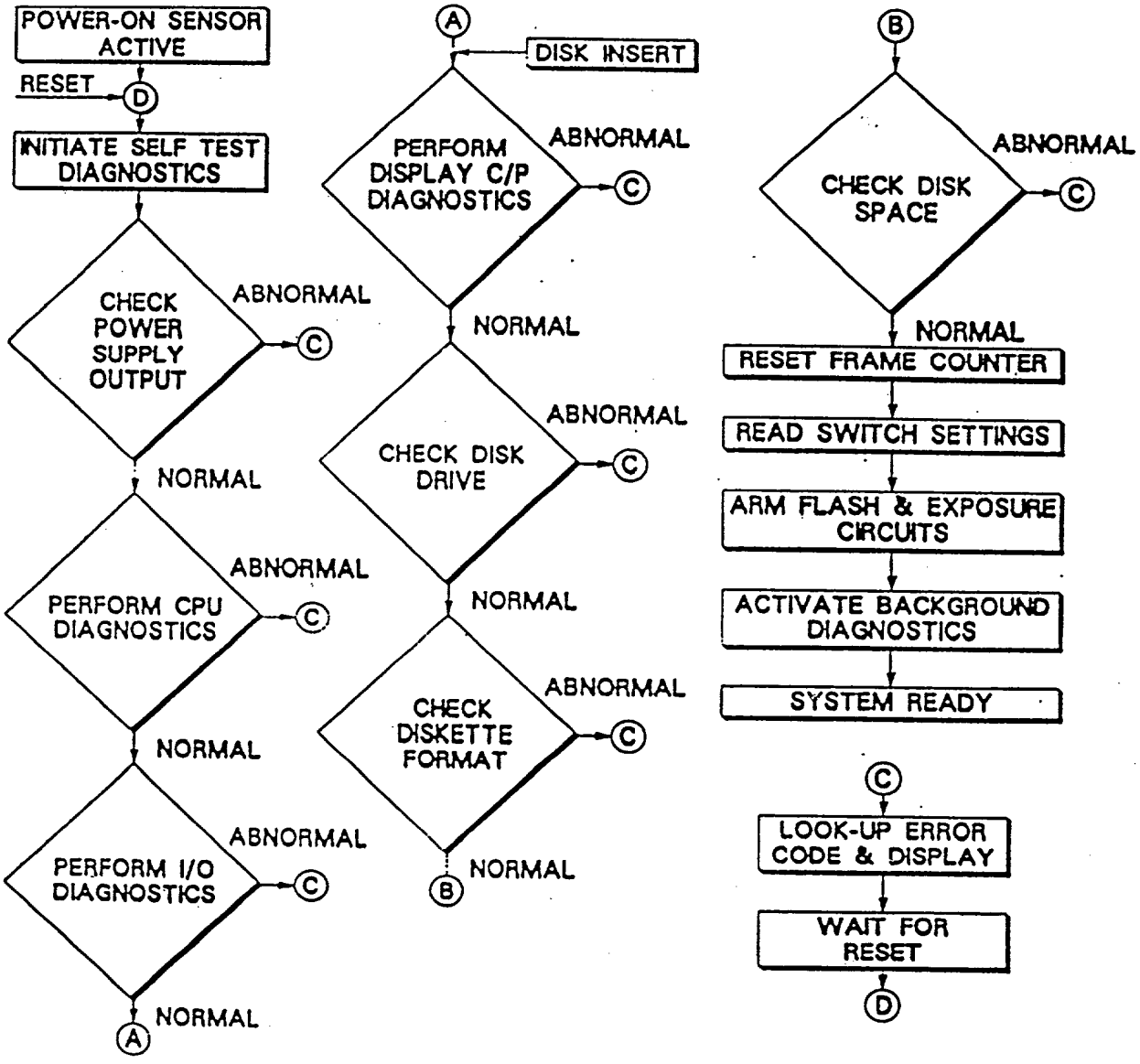
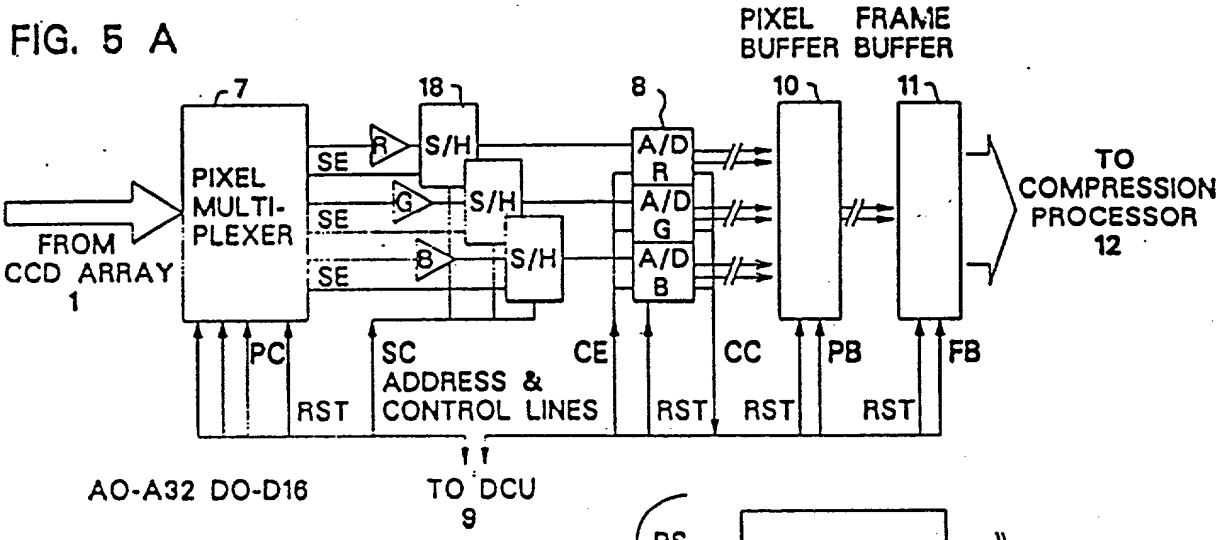

POWER-ON SENSOR ACTIVE
RESET
D
INITIATE SELF TEST DIAGNOSTICS
CHECK POWER SUPPLY OUTPUT
ABNORMAL
C
NORMAL
PERFORM CPU DIAGNOSTICS
ABNORMAL
C
NORMAL
PERFORM I/O DIAGNOSTICS
ABNORMAL
C
NORMAL
A
A
DISK INSERT
PERFORM DISPLAY C/P DIAGNOSTICS
ABNORMAL
C
NORMAL
CHECK DISK DRIVE
ABNORMAL
C
NORMAL
CHECK DISKETTE FORMAT
ABNORMAL
C
NORMAL
B
B
CHECK DISK SPACE
ABNORMAL
C
NORMAL
RESET FRAME COUNTER
READ SWITCH SETTINGS
ARM FLASH & EXPOSURE CIRCUITS
ACTIVATE BACKGROUND DIAGNOSTICS
SYSTEM READY
C
LOOK-UP ERROR CODE & DISPLAY
WAIT FOR RESET
D

FIG. 3

FIG. 5 A



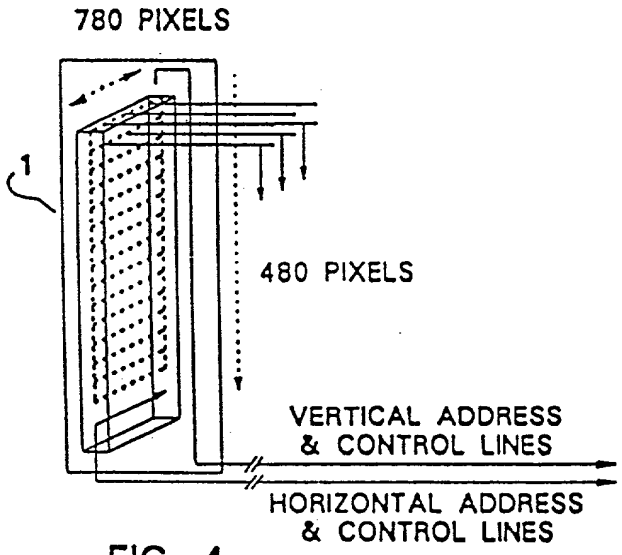




FIG. 4

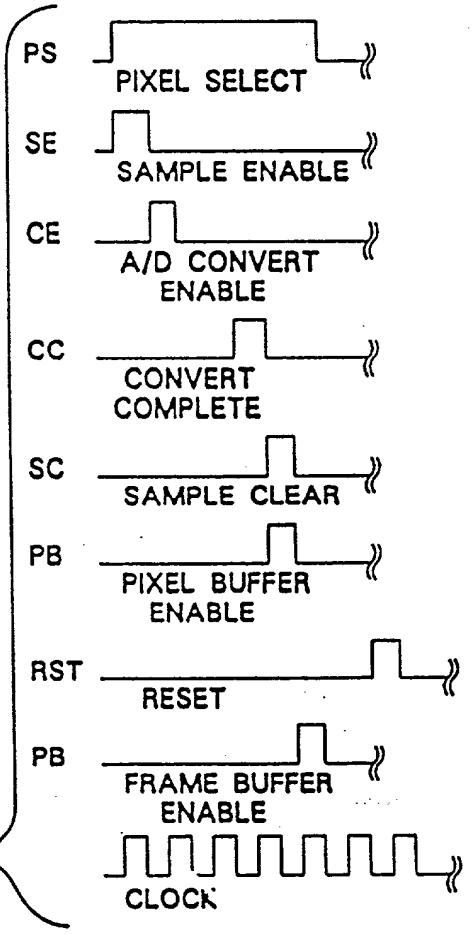



FIG. 5B

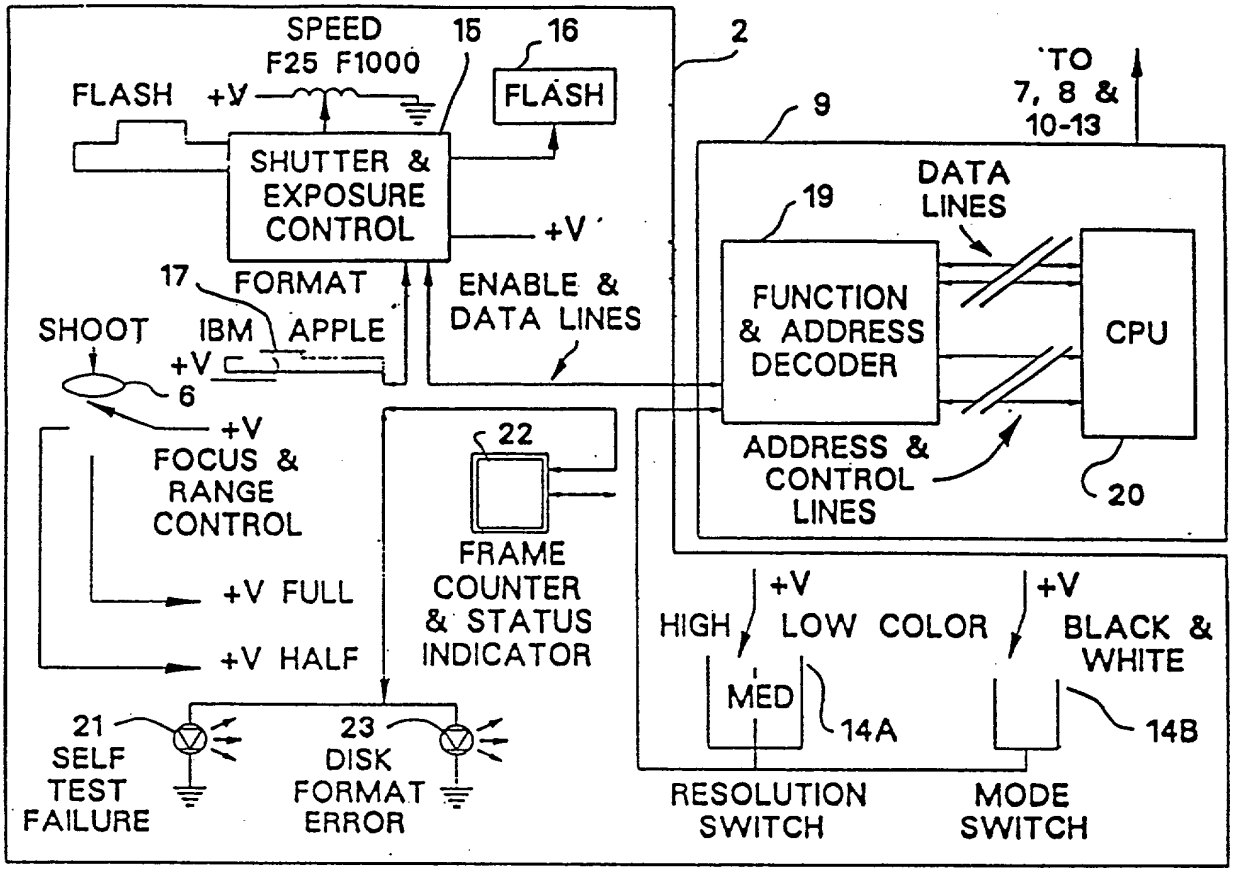



FIG. 6

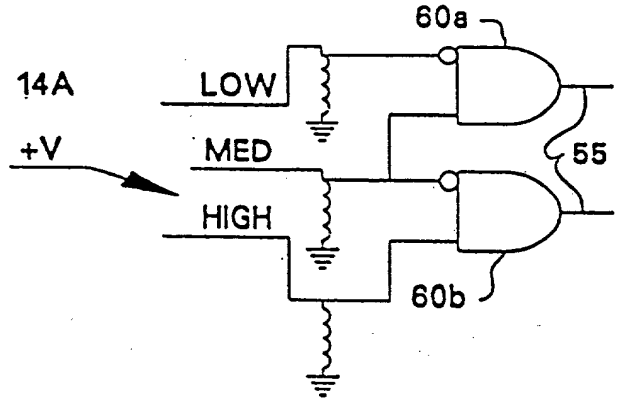



FIG. 6A

| 512-BYTE HEADER |
| --- |
| picSIZE |
| picFRAME |
| OPCODE |
| PICTURE DATA |
| : |
| OPCODE |
| PICTURE DATA END OF PICTURE |

FIG.6B

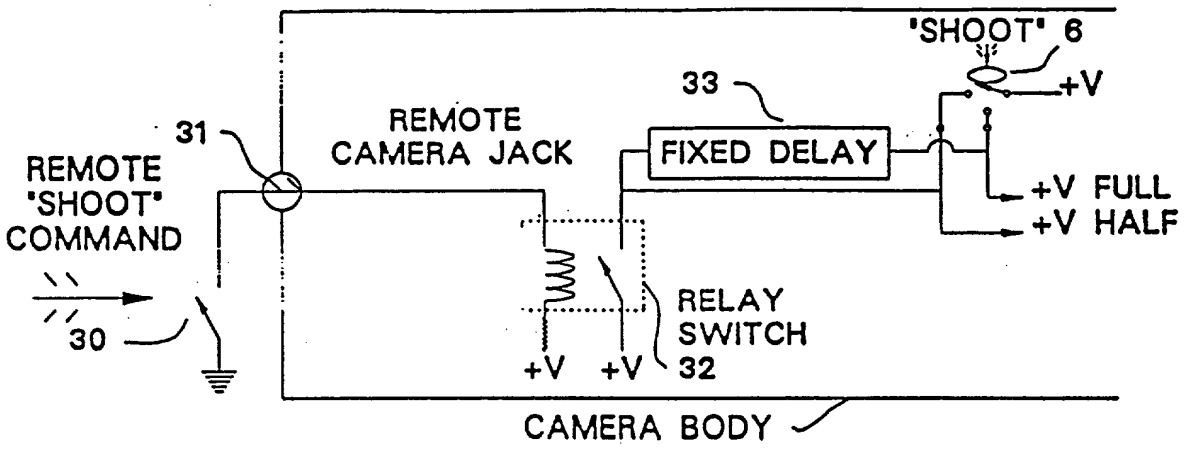

'SHOOT' 6
+V
33
31
REMOTE
CAMERA JACK
FIXED DELAY
REMOTE
'SHOOT'
COMMAND
+V FULL
+V HALF
30
RELAY
SWITCH
+V +V 32
CAMERA BODY

FIG. 6C

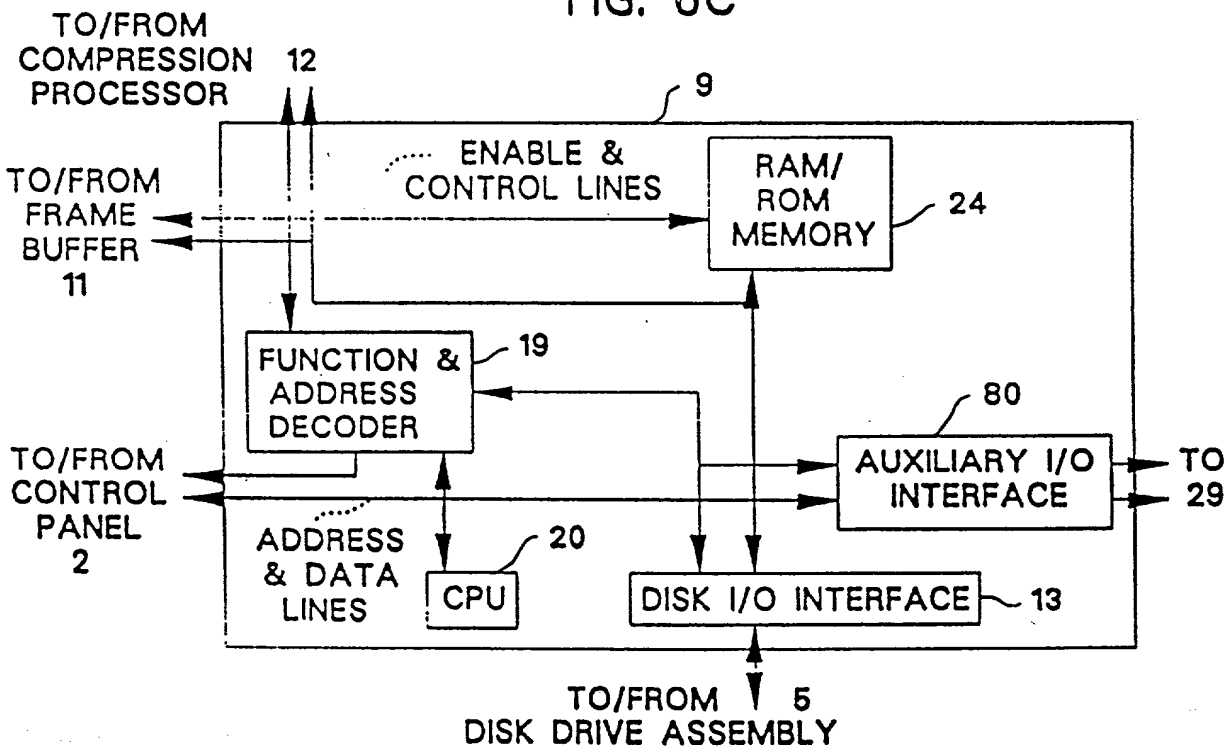

TO/FROM
COMPRESSION
PROCESSOR
12
9
ENABLE &
CONTROL LINES
RAM/
ROM
MEMORY
24
TO/FROM
FRAME
BUFFER
11
FUNCTION &
ADDRESS
DECODER
19
80
AUXILIARY I/O
INTERFACE
TO
29
TO/FROM
CONTROL
PANEL
2
ADDRESS
& DATA
LINES
20
CPU
DISK I/O INTERFACE
13
TO/FROM
DISK DRIVE ASSEMBLY
5

FIG. 7

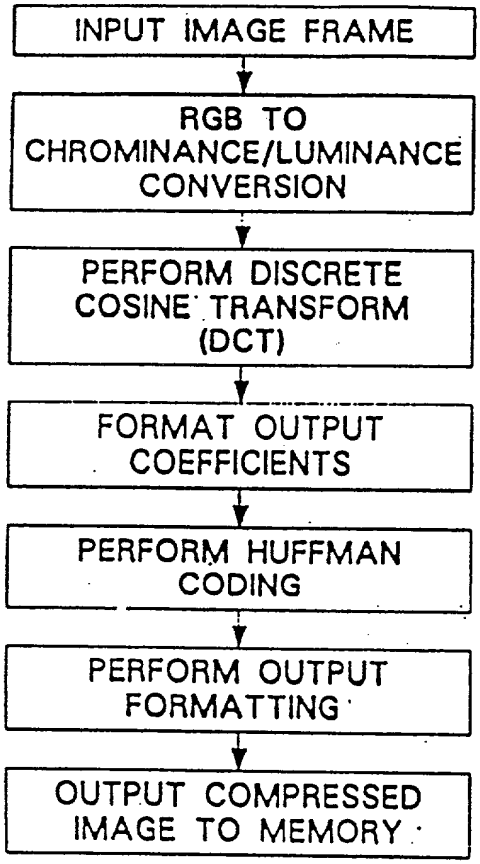



FIG. 8

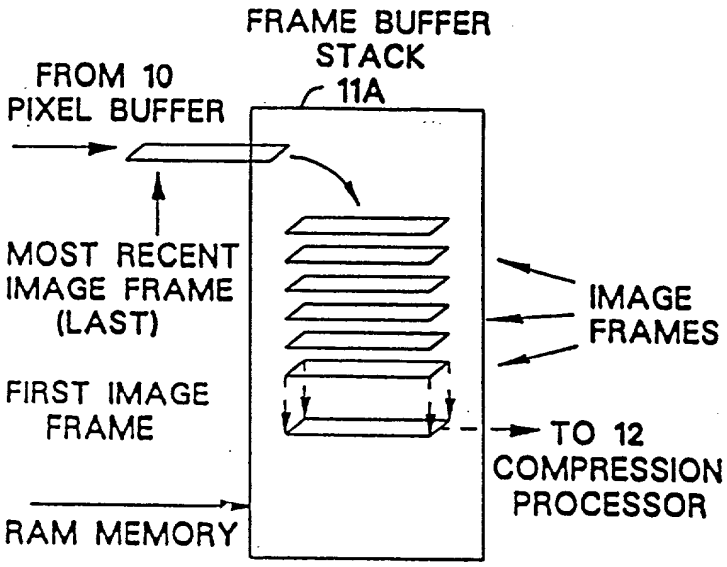



FIG. 13

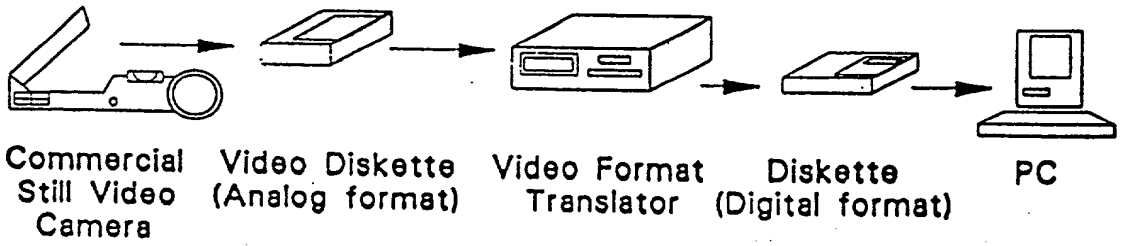



FIG. 10

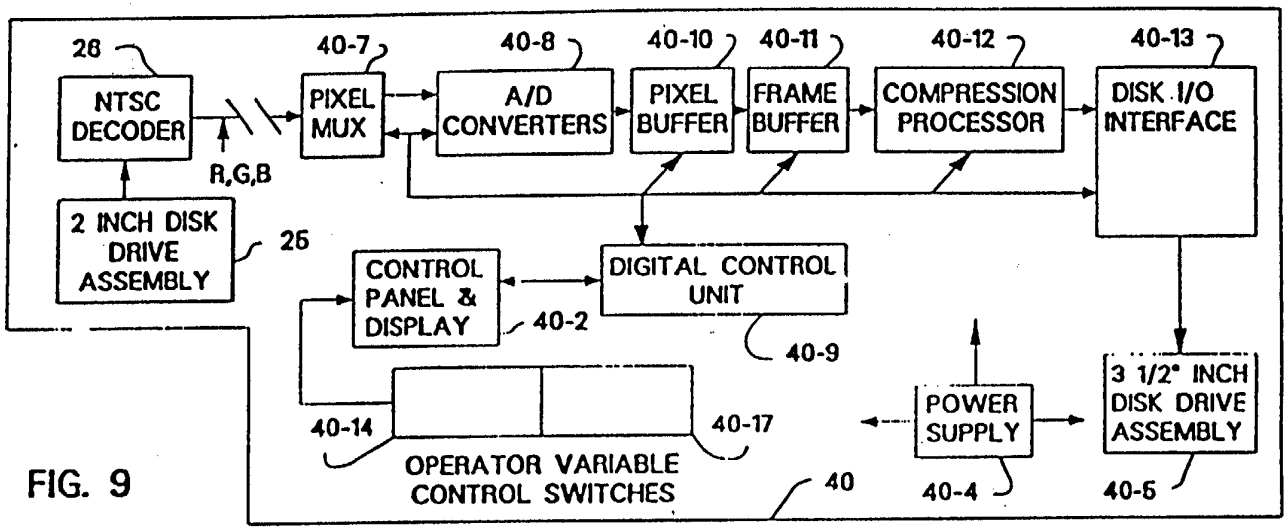

28
NTSC DECODER
R,G,B
2 INCH DISK DRIVE ASSEMBLY
26
40-7
PIXEL MUX
40-8
A/D CONVERTERS
40-10
PIXEL BUFFER
40-11
FRAME BUFFER
40-12
COMPRESSION PROCESSOR
40-13
DISK I/O INTERFACE
CONTROL PANEL & DISPLAY
40-2
DIGITAL CONTROL UNIT
40-9
40-14
40-17
OPERATOR VARIABLE CONTROL SWITCHES
POWER SUPPLY
40-4
3 1/2" INCH DISK DRIVE ASSEMBLY
40-5
40

FIG. 9

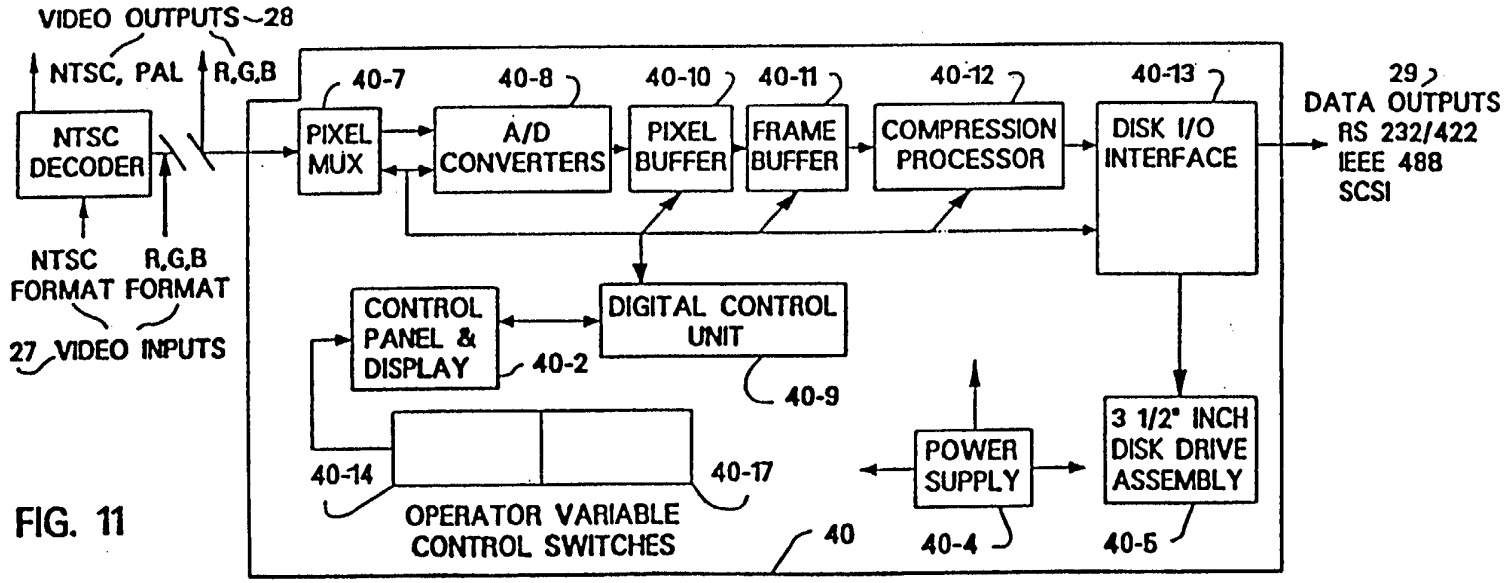

VIDEO OUTPUTS
28
NTSC, PAL
R,G,B
NTSC DECODER
NTSC FORMAT
R,G,B FORMAT
27 VIDEO INPUTS
40-7
PIXEL MUX
40-8
A/D CONVERTERS
40-10
PIXEL BUFFER
40-11
FRAME BUFFER
40-12
COMPRESSION PROCESSOR
40-13
DISK I/O INTERFACE
29
DATA OUTPUTS
RS 232/422
IEEE 488
SCSI
CONTROL PANEL & DISPLAY
40-2
DIGITAL CONTROL UNIT
40-9
40-14
40-17
OPERATOR VARIABLE CONTROL SWITCHES
POWER SUPPLY
40-4
3 1/2" INCH DISK DRIVE ASSEMBLY
40-5
40

FIG. 11

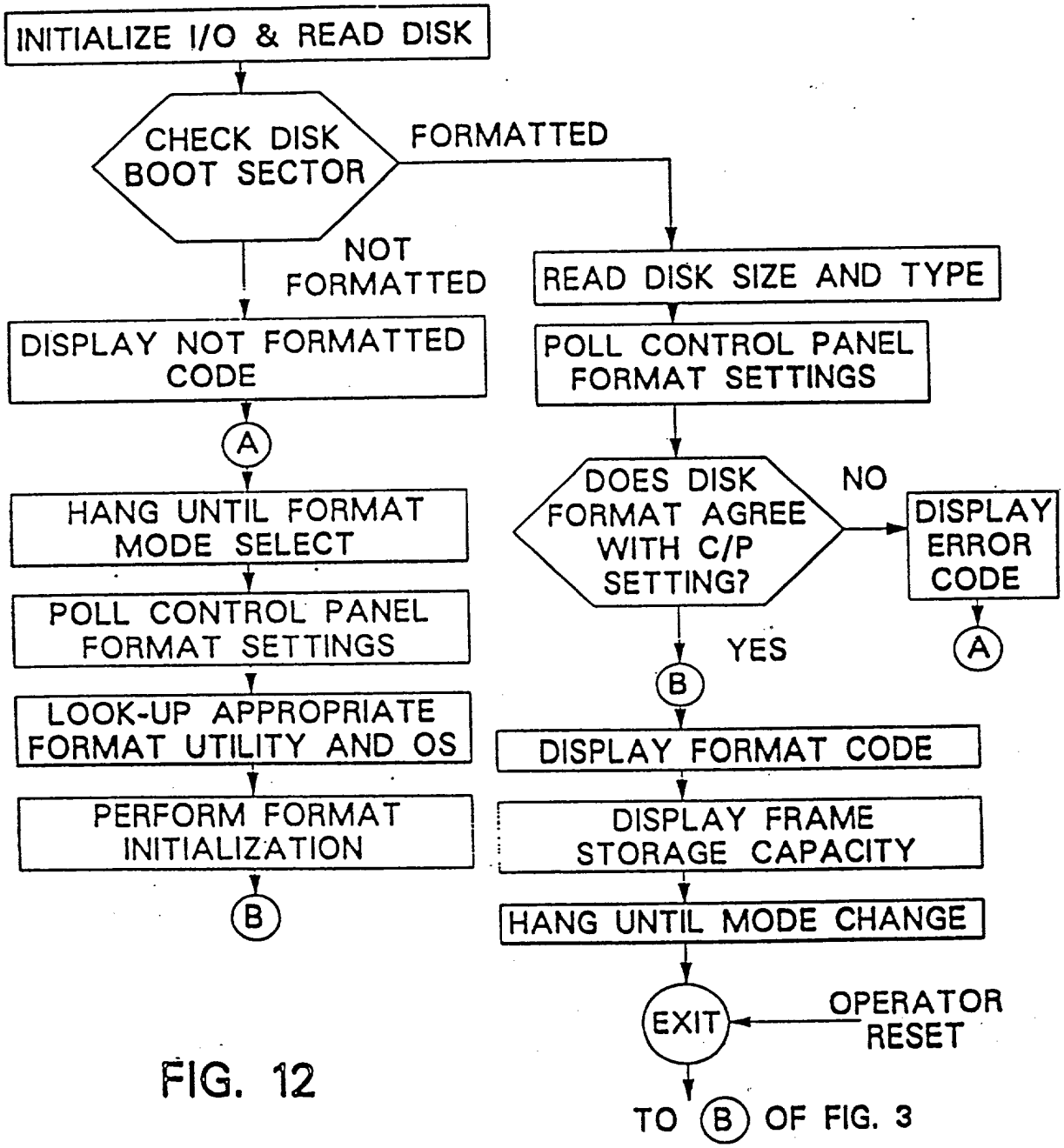

INITIALIZE I/O & READ DISK
CHECK DISK BOOT SECTOR
FORMATTED
NOT FORMATTED
DISPLAY NOT FORMATTED CODE
A
HANG UNTIL FORMAT MODE SELECT
POLL CONTROL PANEL FORMAT SETTINGS
LOOK-UP APPROPRIATE FORMAT UTILITY AND OS
PERFORM FORMAT INITIALIZATION
B
READ DISK SIZE AND TYPE
POLL CONTROL PANEL FORMAT SETTINGS
DOES DISK FORMAT AGREE WITH C/P SETTING?
NO
DISPLAY ERROR CODE
A
YES
B
DISPLAY FORMAT CODE
DISPLAY FRAME STORAGE CAPACITY
HANG UNTIL MODE CHANGE
EXIT
OPERATOR RESET
TO B OF FIG. 3

FIG. 12

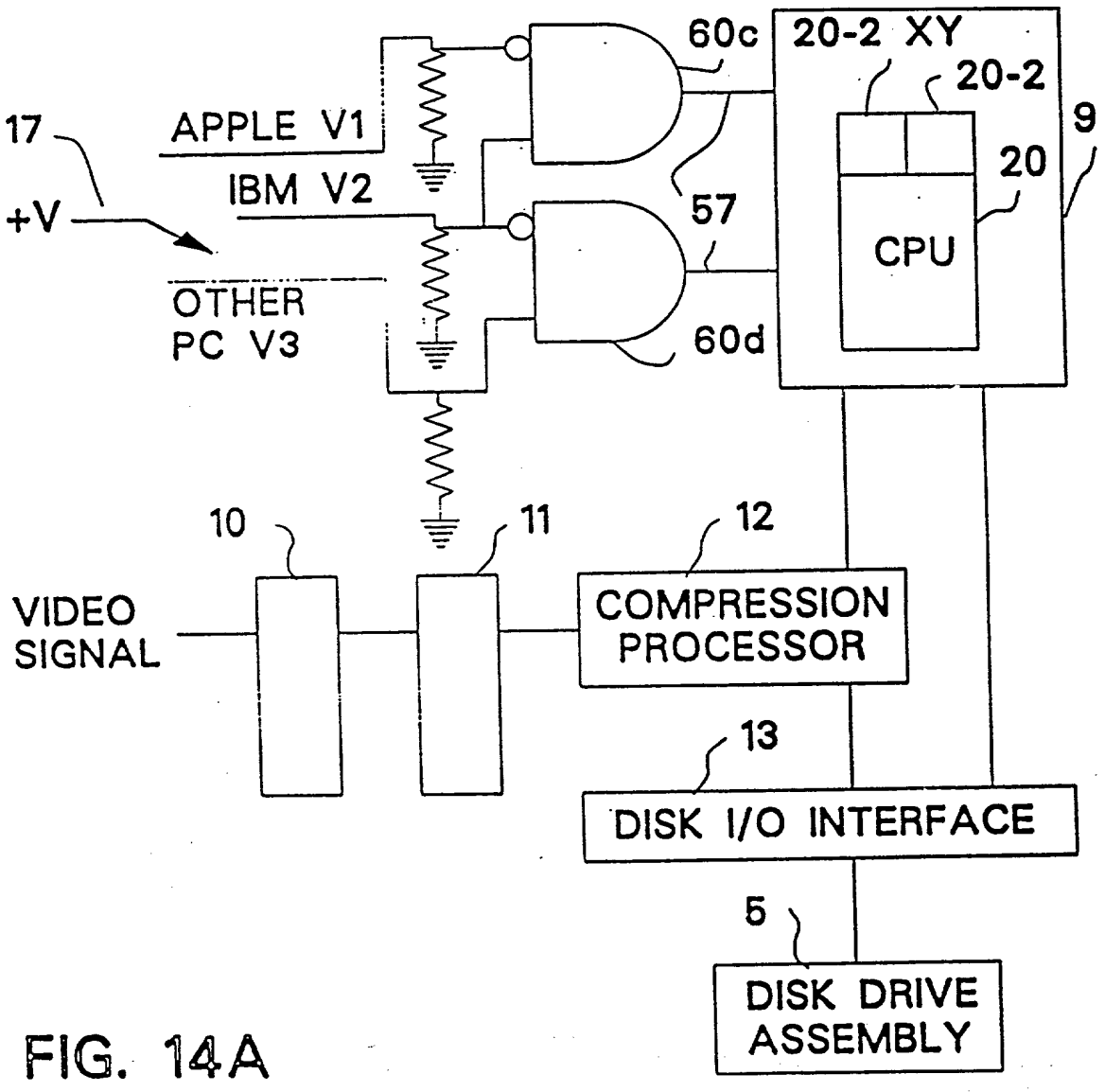

17
+V
APPLE V1
IBM V2
OTHER
PC V3
60c
57
60d
20-2 XY
20-2
20
9
CPU
10
11
12
VIDEO
SIGNAL
COMPRESSION
PROCESSOR
13
DISK I/O INTERFACE
5
DISK DRIVE
ASSEMBLY

FIG. 14A

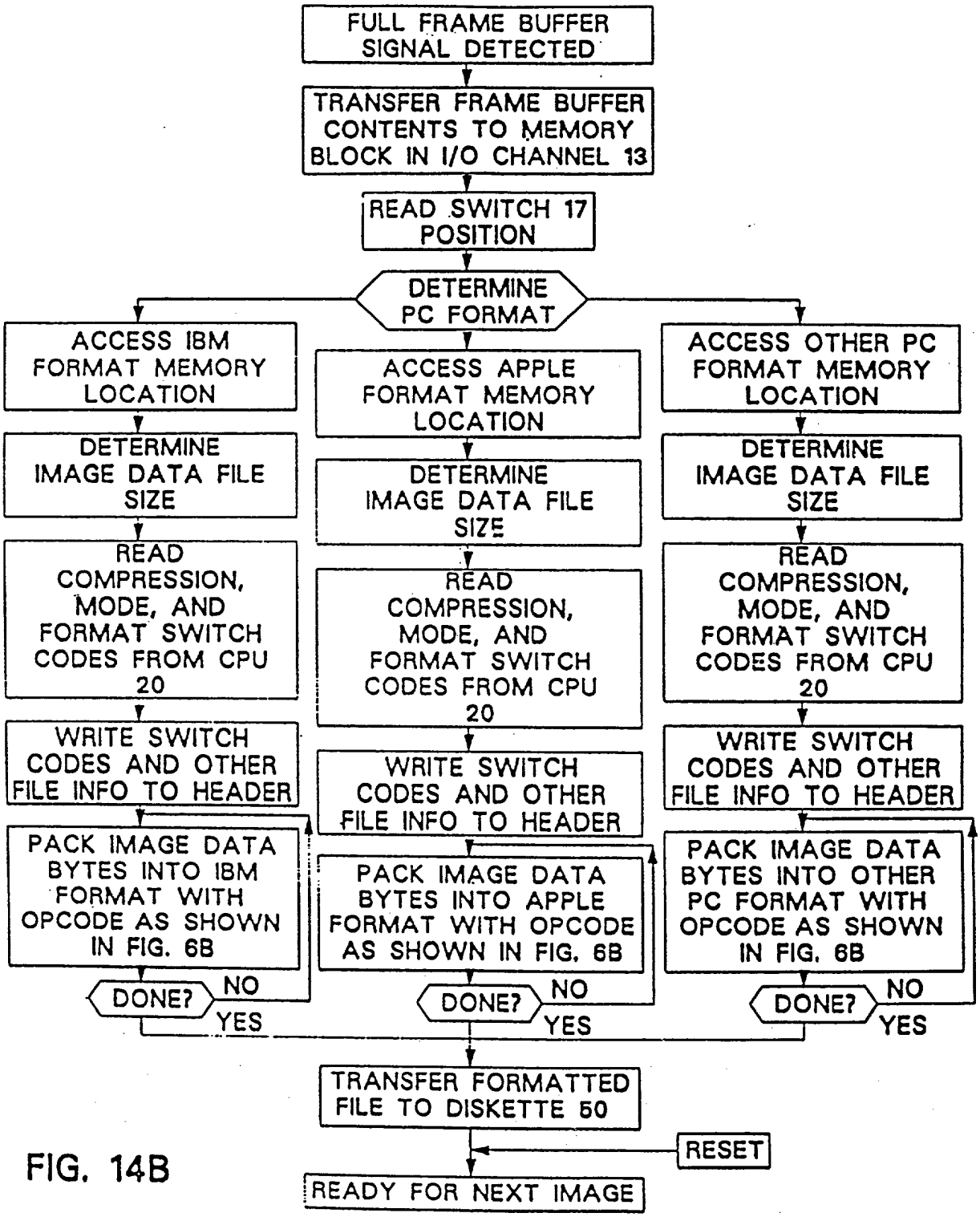

FULL FRAME BUFFER SIGNAL DETECTED
TRANSFER FRAME BUFFER CONTENTS TO MEMORY BLOCK IN I/O CHANNEL 13
READ SWITCH 17 POSITION
DETERMINE PC FORMAT
ACCESS IBM FORMAT MEMORY LOCATION
ACCESS APPLE FORMAT MEMORY LOCATION
ACCESS OTHER PC FORMAT MEMORY LOCATION
DETERMINE IMAGE DATA FILE SIZE
DETERMINE IMAGE DATA FILE SIZE
DETERMINE IMAGE DATA FILE SIZE
READ COMPRESSION, MODE, AND FORMAT SWITCH CODES FROM CPU 20
READ COMPRESSION, MODE, AND FORMAT SWITCH CODES FROM CPU 20
READ COMPRESSION, MODE, AND FORMAT SWITCH CODES FROM CPU 20
WRITE SWITCH CODES AND OTHER FILE INFO TO HEADER
WRITE SWITCH CODES AND OTHER FILE INFO TO HEADER
WRITE SWITCH CODES AND OTHER FILE INFO TO HEADER
PACK IMAGE DATA BYTES INTO IBM FORMAT WITH OPCODE AS SHOWN IN FIG. 6B
PACK IMAGE DATA BYTES INTO APPLE FORMAT WITH OPCODE AS SHOWN IN FIG. 6B
PACK IMAGE DATA BYTES INTO OTHER PC FORMAT WITH OPCODE AS SHOWN IN FIG. 6B
DONE?
NO
YES
DONE?
NO
YES
DONE?
NO
YES
TRANSFER FORMATTED FILE TO DISKETTE 50
RESET
READY FOR NEXT IMAGE

FIG. 14B

***PATENT***

Attorney's Docket No. 101

## COMBINED DECLARATION AND POWER OF ATTORNEY

*(ORIGINAL, DESIGN, NATIONAL STAGE OF PCT, SUPPLEMENTAL, DIVISIONAL, CONTINUATION OR CIP)*

As a below named inventor, I hereby declare that:

### TYPE OF DECLARATION

This declaration is of the following type: (*check one applicable item below*)

- [X] original
- [ ] design

*NOTE: If the declaration is for an International Application being filed as a divisional, continuation or continuation-in-part application do not check any of next two items and check appropriate one of last three items.*

- [ ] national stage of PCT
- [ ] supplemental

*NOTE: If one of the following 3 items apply then complete and also attach ADDED PAGES FOR DIVISIONAL, CONTINUATION OR CIP.*

- [ ] divisional
- [ ] continuation
- [ ] continuation-in-part (CIP)

### INVENTORSHIP IDENTIFICATION

***WARNING:*** *If the inventors are each not the inventors of all the claims an explanation of the facts, including the ownership of all the claims at the time the last claimed invention was made, should be submitted.*

My residence, post office address and citizenship are as stated below next to my name, I believe I am the original, first and sole inventor (*if only one name is listed below*) or an original, first and joint inventor (*if plural names are listed below*) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

### TITLE OF INVENTION

ELECTRONIC STILL VIDEO CAMERA WITH DIRECT PERSONAL COMPUTER(PC) COMPATIBLE DIGITAL FORMAT OUTPUT

### SPECIFICATION IDENTIFICATION

the specification of which: *(complete (a), (b) or (c))*

(a) [X] is attached hereto.

(b) [ ] was filed on _____ as [ ] Serial No. _____ or [ ] Express Mail No., *as Serial No. not yet known* _____ and was amended on _____ (*if applicable*).

*NOTE: Amendments filed after the original papers are deposited with the PTO which contain new matter are not accorded a filing date by being referred to in the declaration. Accordingly, the amendments involved are those filed with the application papers or, in the case of a supplemental declaration, are those amendments claiming matter not encompassed in the original statement of invention or claims. See 37 CFR 1.67.*

(c) ☐ was described and claimed in PCT International Application No. _____ filed on _____ and as amended under PCT Article 19 on _____ (*if any*).

**ACKNOWLEDGEMENT OF REVIEW OF PAPERS AND DUTY OF CANDOR**

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations. § 1.56(a).

☐ In compliance with this duty there is attached an information disclosure statement. 37 CFR 1.97. TO BE FILED LATER

**PRIORITY CLAIM**

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed.

*(complete (d) or (e))*

(d) ☐ no such applications have been filed.

(e) ☐ such applications have been filed as follows

*NOTE: Where item (c) is entered above and the International Application which designated the U.S. claimed priority check item (e), enter the details below and make the priority claim.*

**EARLIEST FOREIGN APPLICATION(S), IF ANY FILED WITHIN 12 MONTHS (6 MONTHS FOR DESIGN) PRIOR TO THIS U.S. APPLICATION**

| COUNTRY | APPLICATION NUMBER | DATE OF FILING (month, day, year) | PRIORITY CLAIMED UNDER 37 USC 119 |
|---|---|---|---|
| | | | ☐YES NO☐ |
| | | | ☐YES NO☐ |
| | | | ☐YES NO☐ |
| | | | ☐YES NO☐ |
| | | | ☐YES NO☐ |

**ALL FOREIGN APPLICATION(S), IF ANY FILED MORE THAN 12 MONTHS (6 MONTHS FOR DESIGN) PRIOR TO THIS U.S. APPLICATION**

_____

_____

_____

## POWER OF ATTORNEY

As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (*List name and registration number*)

PAUL W. FISH
REG # 22435 201

SEND CORRESPONDENCE TO

PAUL W. FISH
SUITE 410
4200 MASSACHUSETTS AVE NW
WASHINGTON DC 20016

DIRECT TELEPHONE CALLS TO:
(*Name and telephone number*)

PAUL W. FISH
202 363-6263

## DECLARATION

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

## SIGNATURE(S)

Full name of **sole or first inventor** MARC K. ROBERTS 40100
Inventor's signature Marc K. Roberts
Date 20 NOV 1990 Country of Citizenship USA
Residence 5701 WOODEN HAWK LANE BURKE, VA. 22015
Post Office Address SAME AS RESIDENCE 11A

Full name of **second joint inventor, if any** MATTHEW A. CHIKOSKY 40200
Inventor's signature Matthew A. Chikosky
Date 20 NOV 1990 Country of Citizenship USA
Residence 7388 SHADY PALM DR. SPRINGFIELD VA. 22153
Post Office Address SAME AS RESIDENCE 11A

## ADDED PAGE TO COMBINED DECLARATION AND POWER OF ATTORNEY FOR SIGNATURE BY THIRD AND SUBSEQUENT INVENTORS

Full name of third joint inventor, if any JERRY A. SPEASL 40430

Inventor's signature Jerry A. Speasl

Date 20NOV 1990 Country of Citizenship USA

Residence 10727 HUNTERS PLACE VIENNA VA. 22180 VA

Post Office Address SAME AS RESIDENCE

Full name of fourth joint inventor, if any

Inventor's signature

Date Country of Citizenship

Residence

Post Office Address

Full name of fifth joint inventor, if any

Inventor's signature

Date Country of Citizenship

Residence

Post Office Address